Activity 2.4.2

Introduction to Programmable Logic Devices (PLD) Using PLTW S7

INTRODUCTION

When circuit designs become too large or complex to realistically breadboard, designers often use a **Programmable Logic Device (PLD)** to prototype and test a circuit. A PLD is an **integrated circuit** whose logic function is user-configurable. Unlike discrete logic gates—such as the AND, OR, NAND, and NOR gates, whose functionality is fixed when they are manufactured—a PLD must be programmed before use.

The first user-configurable PLD was introduced in 1978. This PLD was called a Programmable Array Logic (PAL), and it contained 24 user input/output signals. Over the decades since the PAL was first introduced, the complexity of the devices and level of integration has increased significantly. The current state-of-the-art for PLDs is the **Field Programmable Gate Array (FPGA)**. The FPGA referenced in this activity is the PLTW S7.

In this activity, you will learn how to use the Circuit Design Software (CDS) to program the FPGA on the Digital MiniSystem (DMS).

EQUIPMENT

These instructions are for use with the PLTW S7 module shown. If you do not have the PLTW S7 then ask your teacher to guide you to the correct activity. These instructions assume that all necessary software has been installed and configured for this course.

PLTW S7 Module

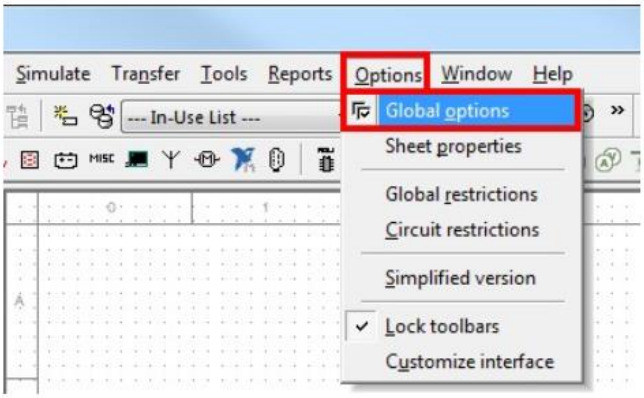
- Digital MiniSystem (DMS)
- Programmable logic device (PLTW S7 FPGA Module)
- Computer with the following software
  - Circuit Design Software (CDS) such as Multisim 14
  - Xilinx Programming Software (XPS)

Procedure

Part 1: Setting Up the CDS (Multisim) in PLD Mode

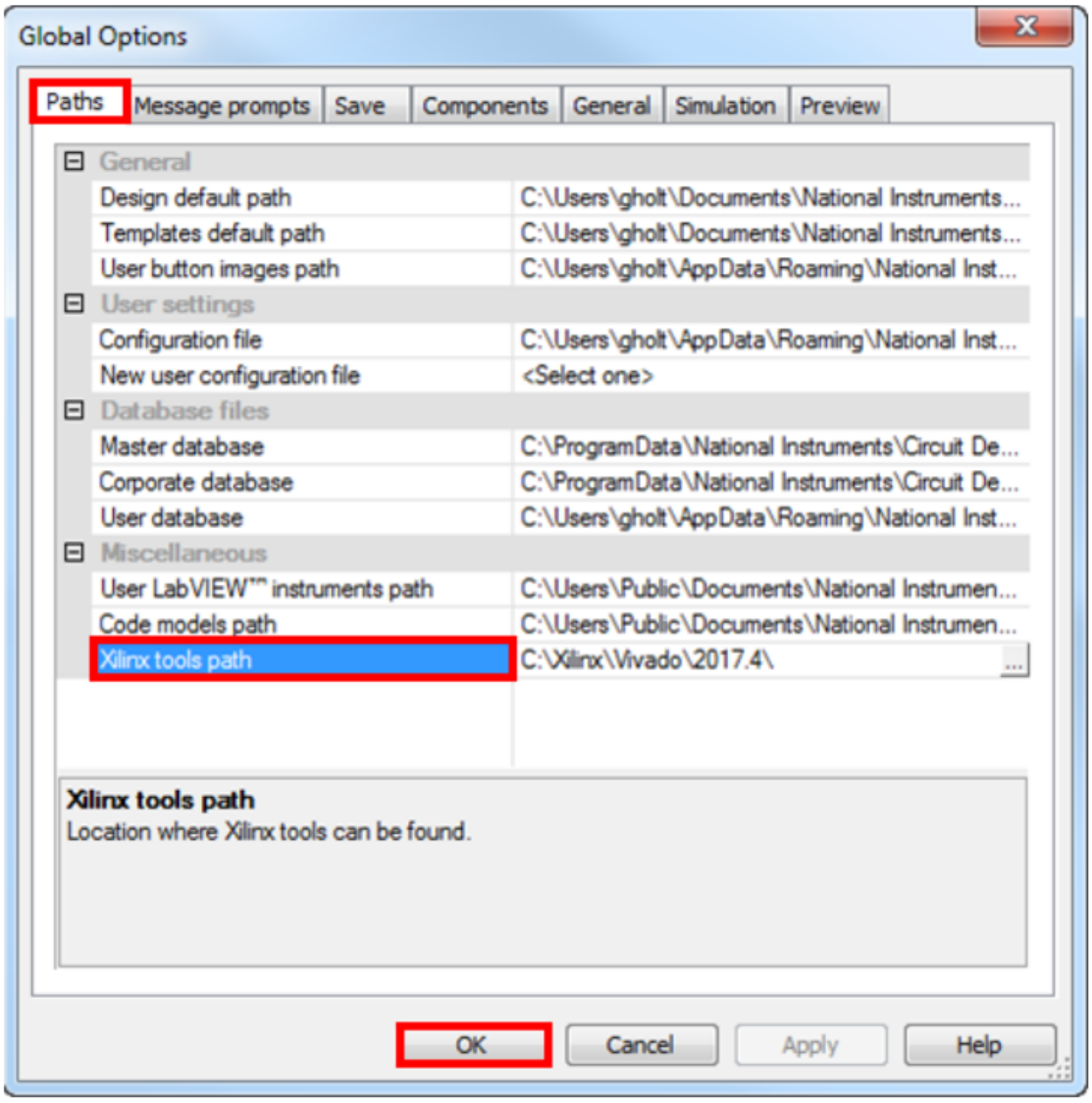
1. Start the **CDS** software.

   Select **Options** > **Global options** to open the the dialog box.



2. Select the **Paths** tab > **Xilinx tools path** under **Miscellaneous** section. Confirm that Xilinx tools path is set to the path shown. **C:\Xilinx\Vivado\2017.4**

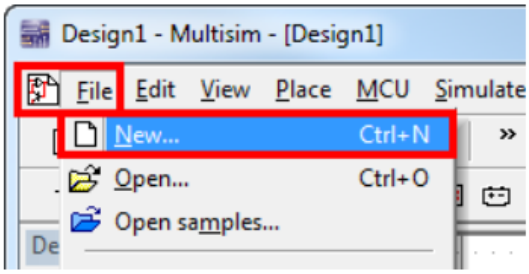
> **Note**: Your instructor may provide a different path for you to use.



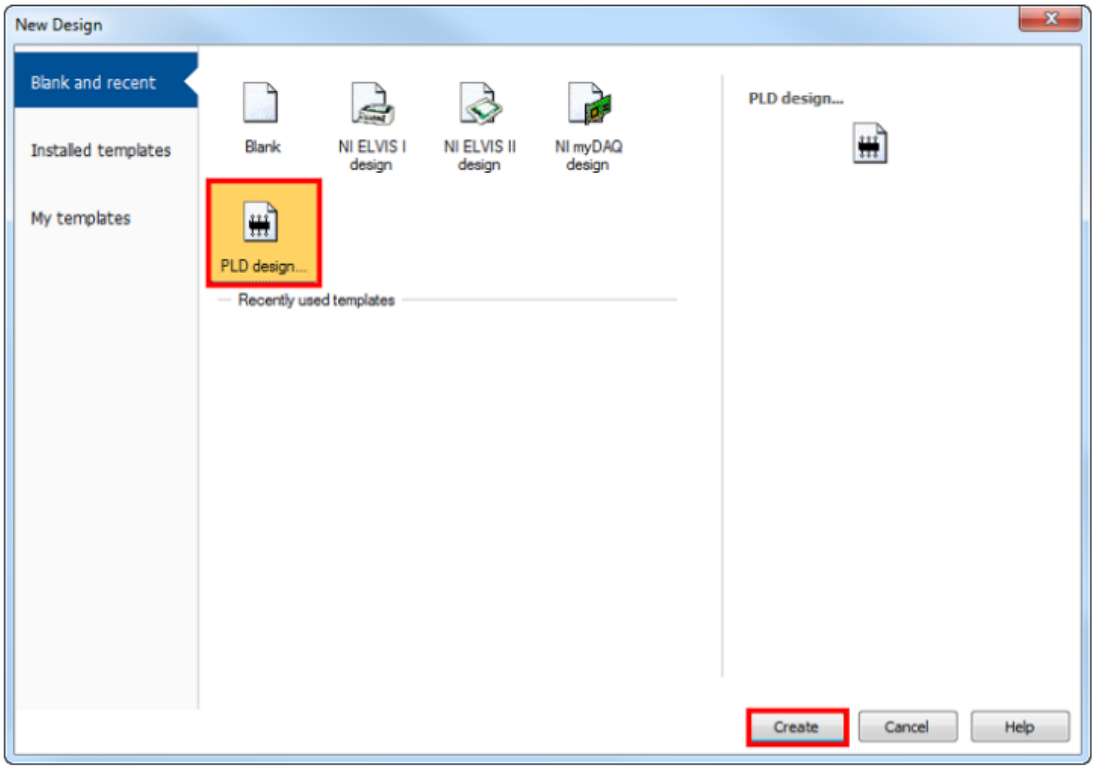
3. Select **OK**. This is a one-time setup, which your instructor may have already completed.

4. **Create** a new folder called **Tutorial** in a location which you typically have access.

5 From the CDS software select **File** > **New (Ctrl+N)**.



This will open the File Wizard. Select **PLD design** > **Create**.

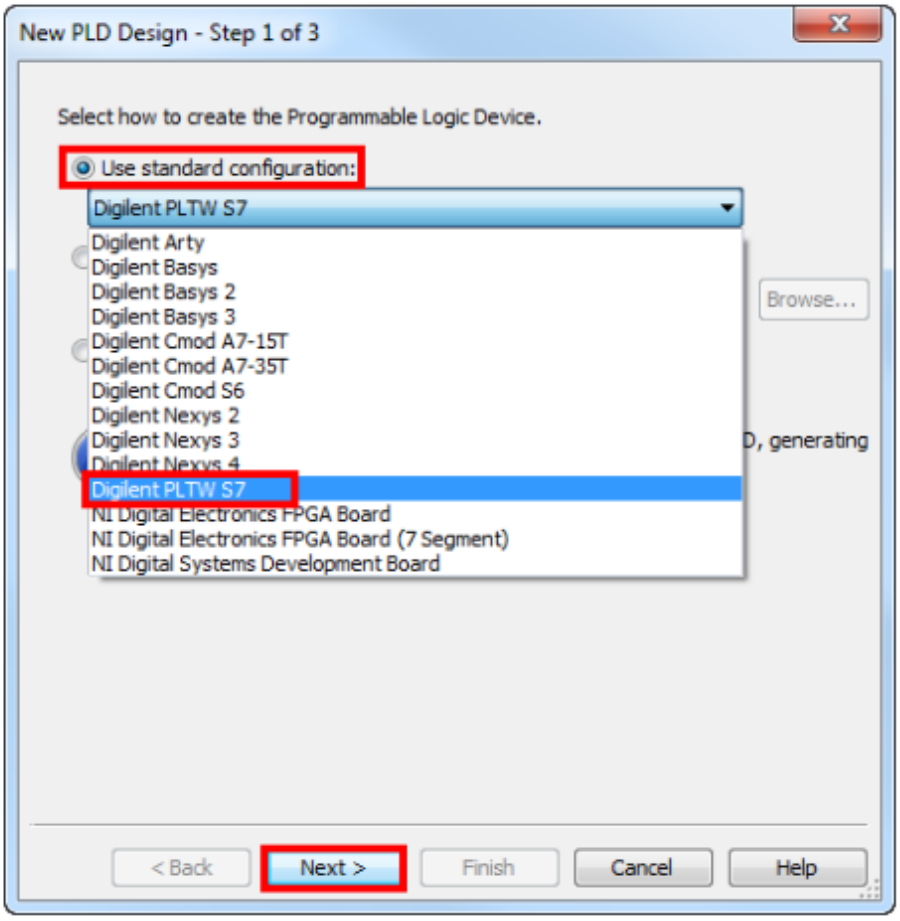


6 New PLD Design – Step 1 of 3:

a. Select **Use standard configuration**.

b. Select Digilent PLTWS7

c. Select **Next**.

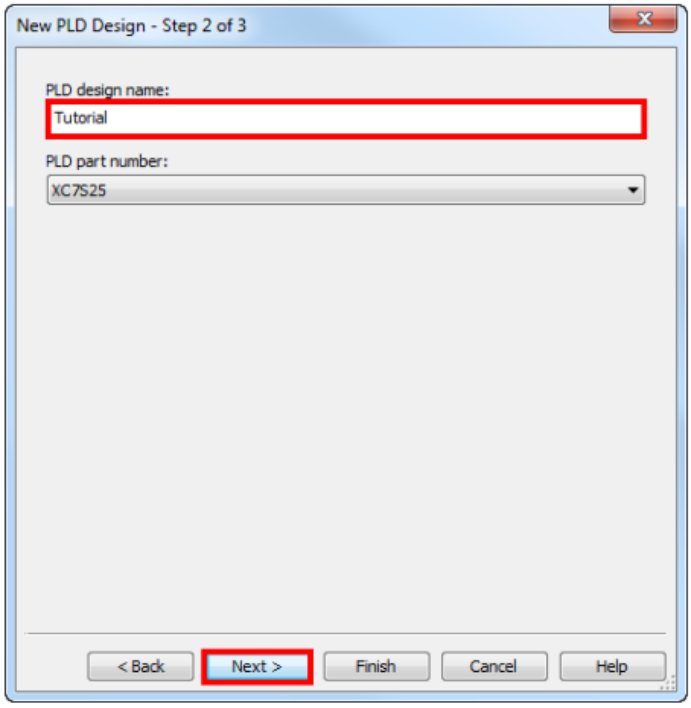


7 New PLD Design – Step 2 of 3:

a. Enter **Tutorial** in the **PLD Design name** field.

b. Select **Next**.

> **Note**: The XPS, which you will use later in this tutorial, does not accept numbers, spaces, and some special characters in file names. Select **Next**.

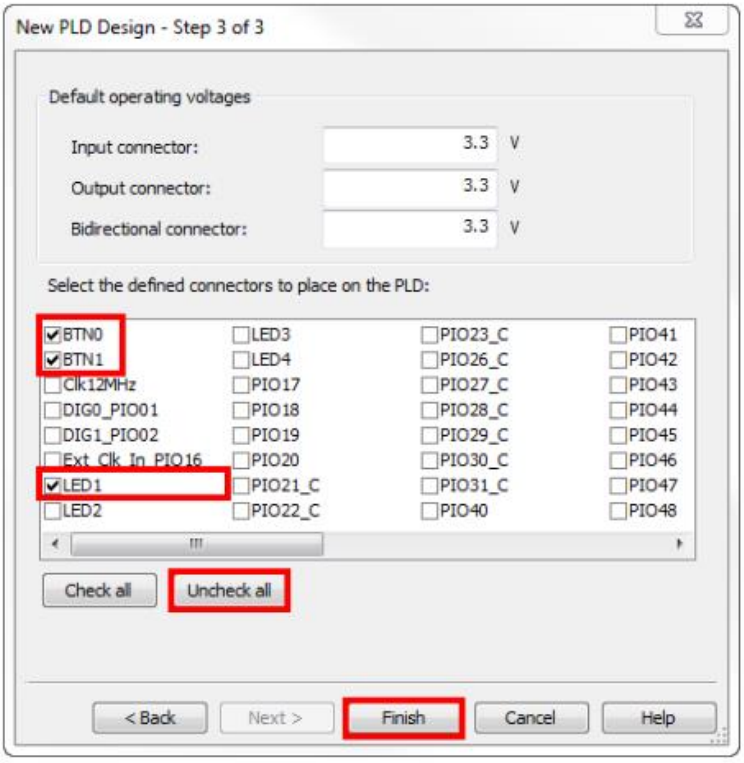


8 New PLD Design – Step 3 of 3:

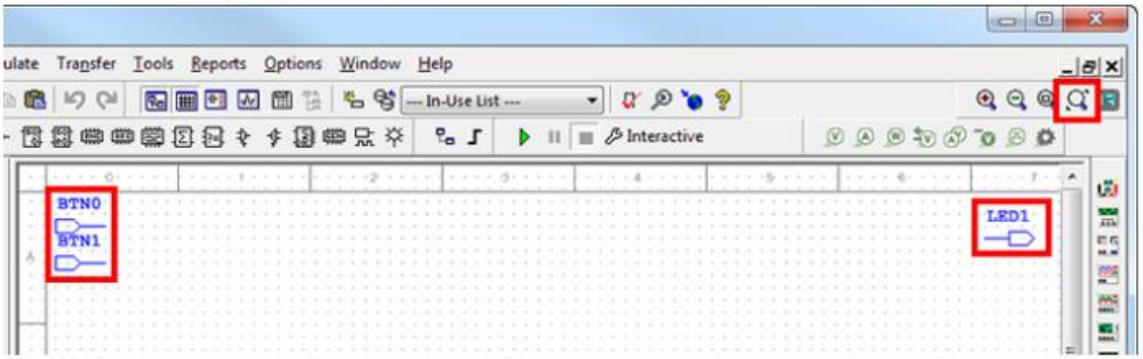
For this example, we will program a simple OR gate.

A. Select **Uncheck all** and then individually select the desired connectors. Use **btn0**, **btn1**, and **led1**.

B. Select **Finish**.



The CDS opens a sheet in PLD mode with two port connectors on the left (the buttons) and one on the right (the LED). Use the **Zoom Sheet** icon to show the entire sheet.

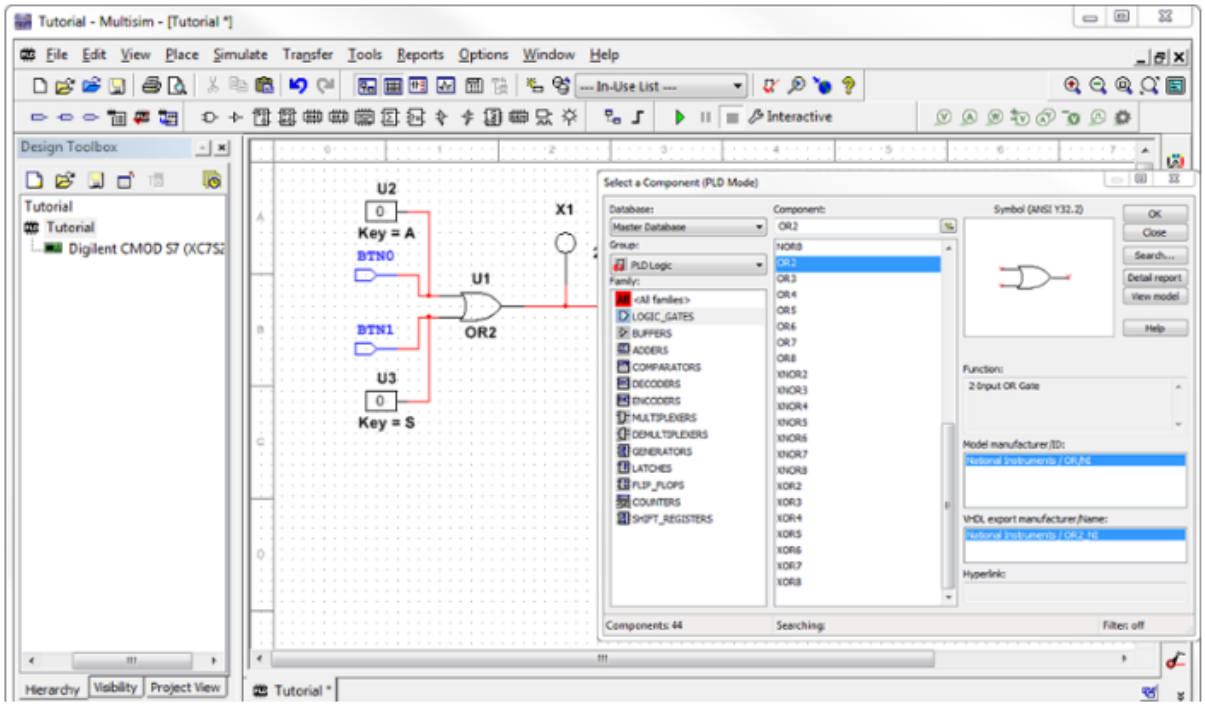


- To remove a port connector, simply delete it.
- To add a port connector, select **Place** > **Connector**. Then choose the appropriate connector for the design.
- To change port connector name and function (Mode), right-click a connector and choose **Properties**.
- To ignore the error message that follows a change, select **YES**.

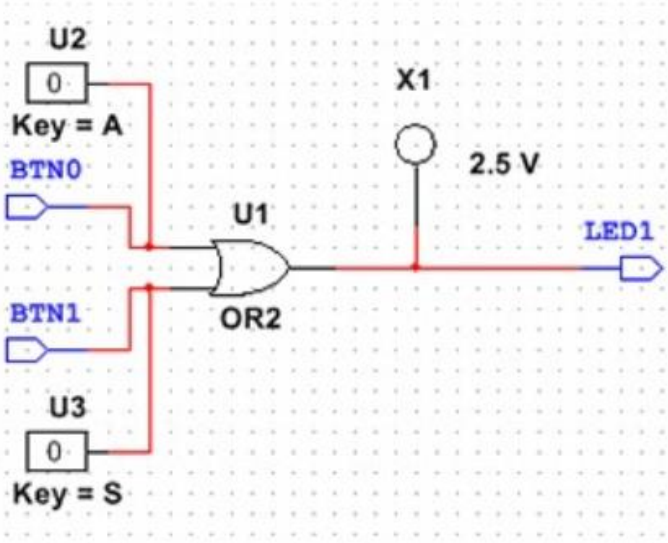
Part 2: Simulating a PLD Mode Design in the CDS (Multisim)

The PLD Mode includes a different list of components than you used in the Design Mode. Components from one mode do not work in the other; however, use the simulation feature within PLD Mode to test whether the circuit is working before you program the DLB.

Components are found and placed in **PLD Mode** the same way they were in **Design Mode**. The PLD logic components are generic so these do not include part numbers.



12 Create the circuit shown.



A. Move the btn0, btn1, and led1 into their approximate position.

B. Place an OR gate using either of the steps shown.

I. Select the **Place Logic Gate** icon > **PLD Logic** group > **OR2** > **OK**. Position the gate then connect the wires.

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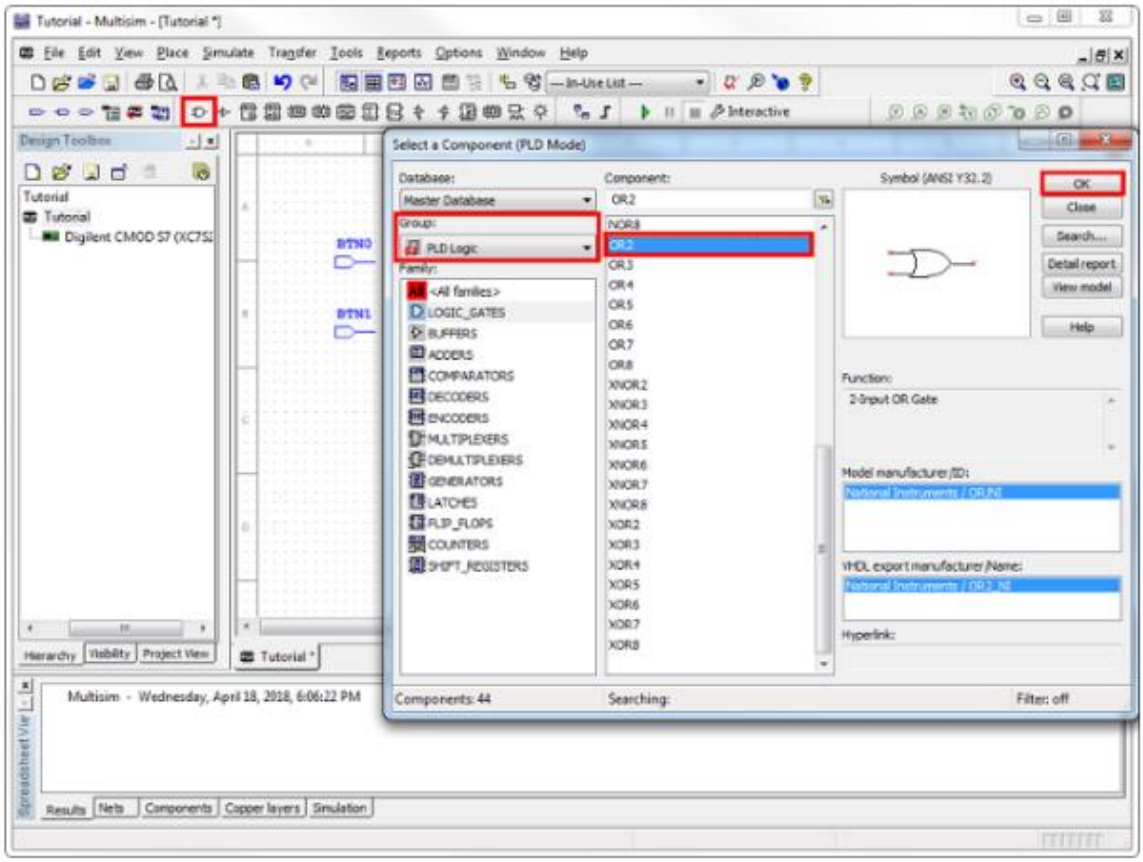
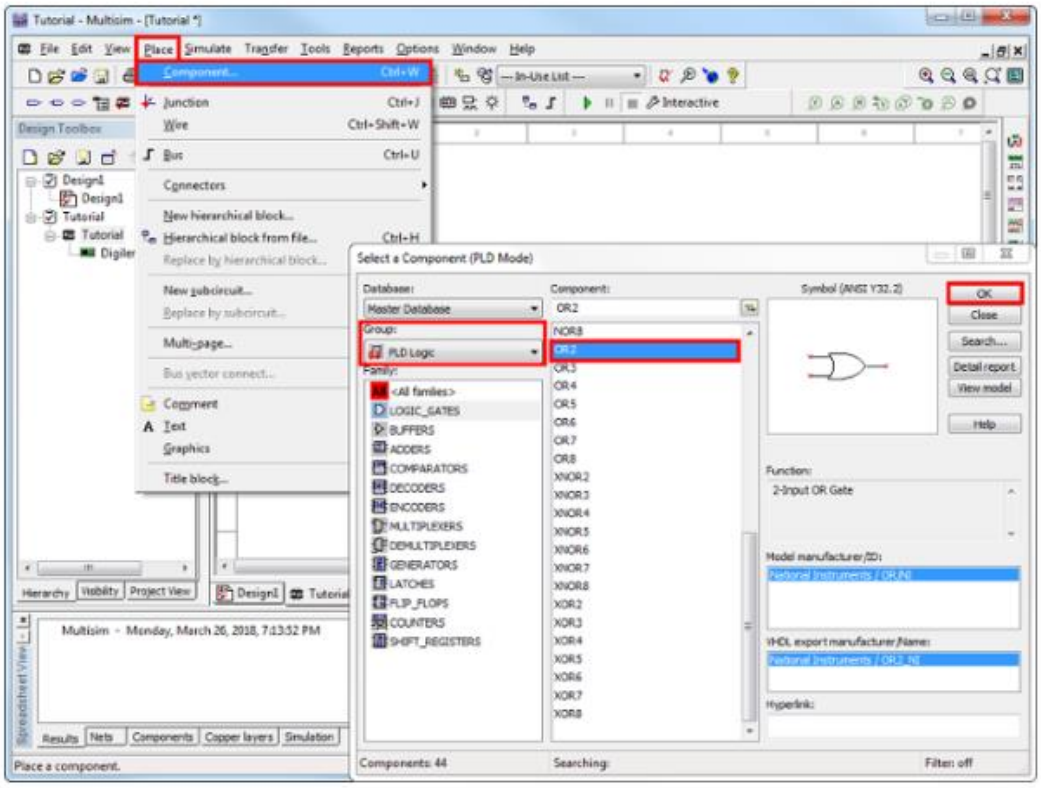
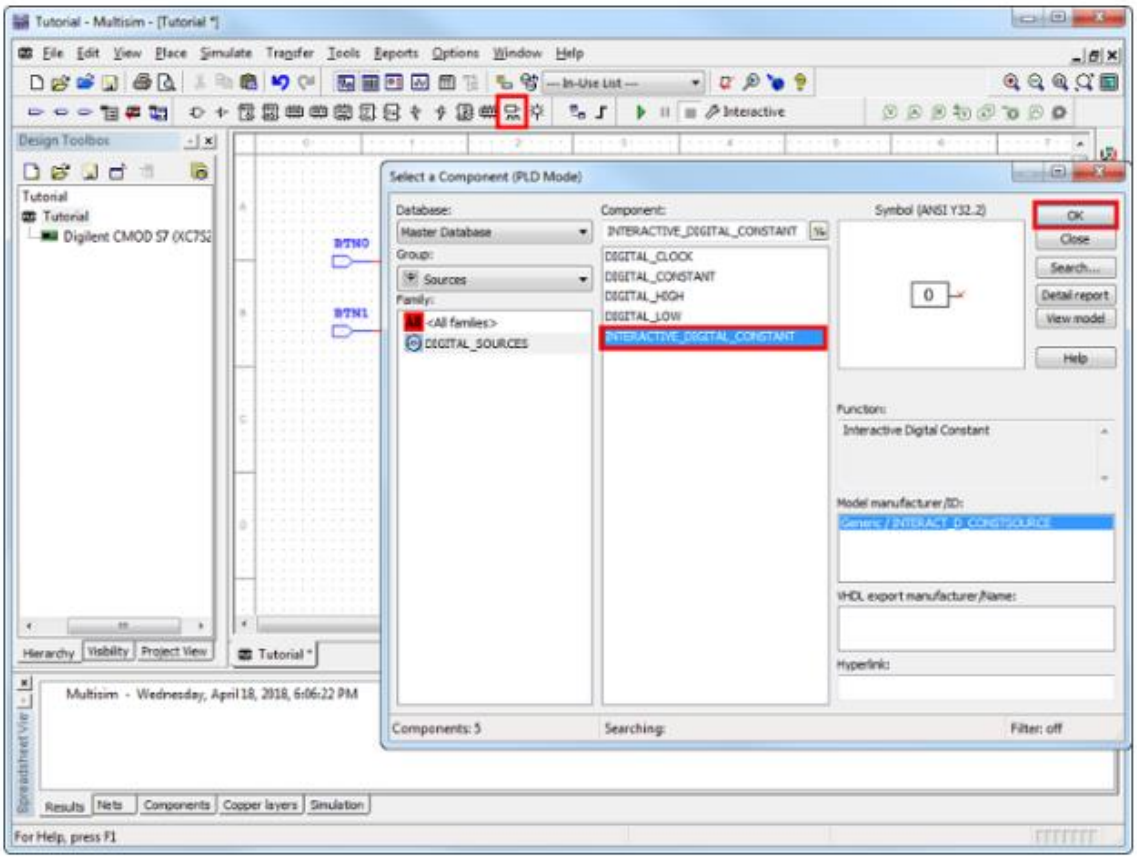


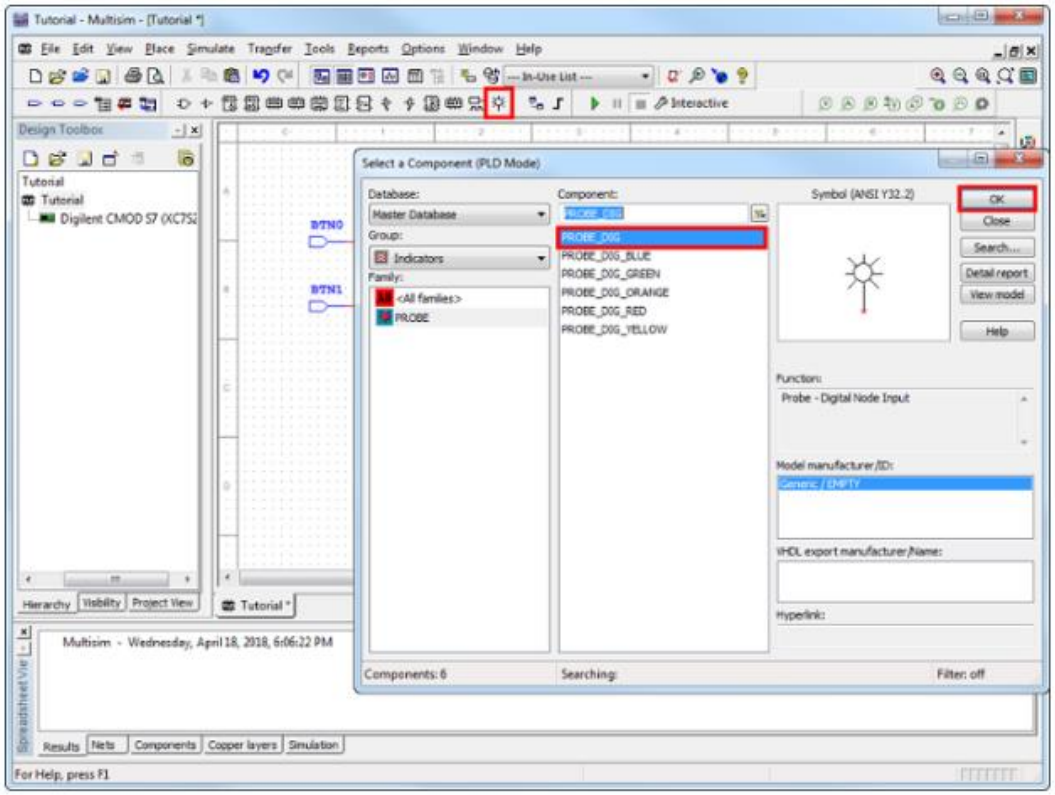
II. Select **Place** > **Component** > **PLD Logic** group > **OR2** > **OK**. Position the gate then connect the wires.



C. Select **Place digital source** icon > **INTERACTIVE_DIGITAL_CONSTANT** > **OK**. Do this again to create a second digital source. Position the sources then connect the wires. Change the keyboard input options.

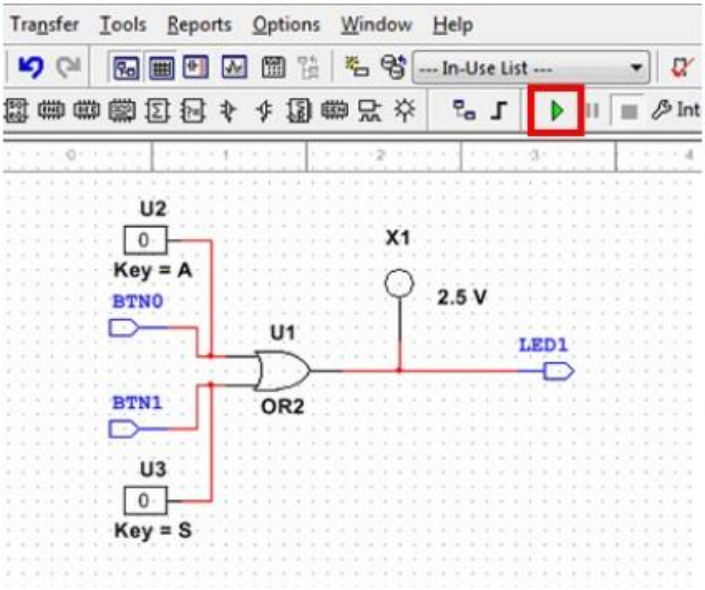


D. Select **Place probe** icon > **PROBE_DIG** > **OK**. Position the probe then connect the wire.



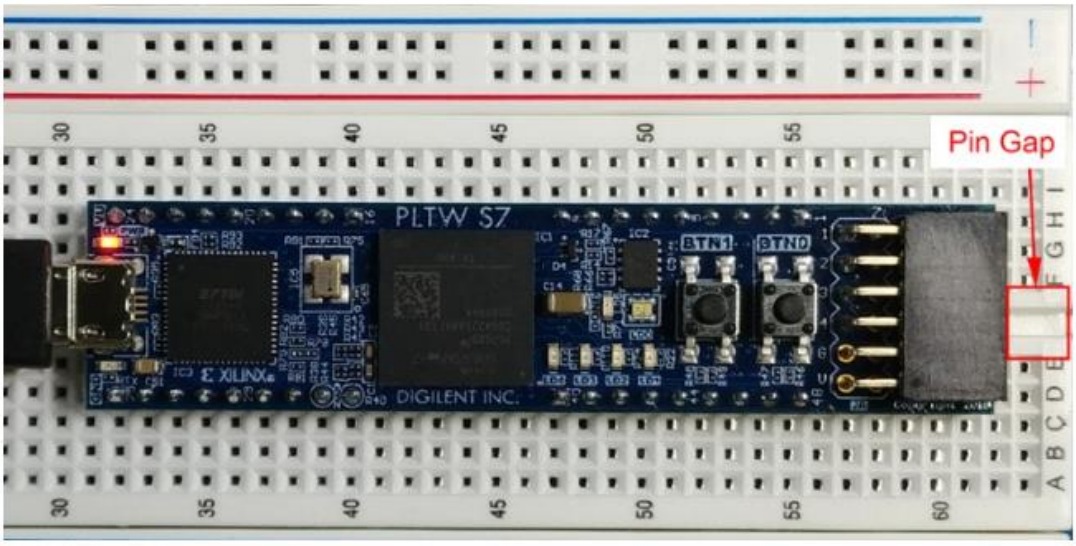
13 Save the circuit to the Tutorial project folder you created.

14 From the simulation toolbar, select the **Run** icon or F5 on the keyboard. Verify that the circuit functions correctly before exporting.

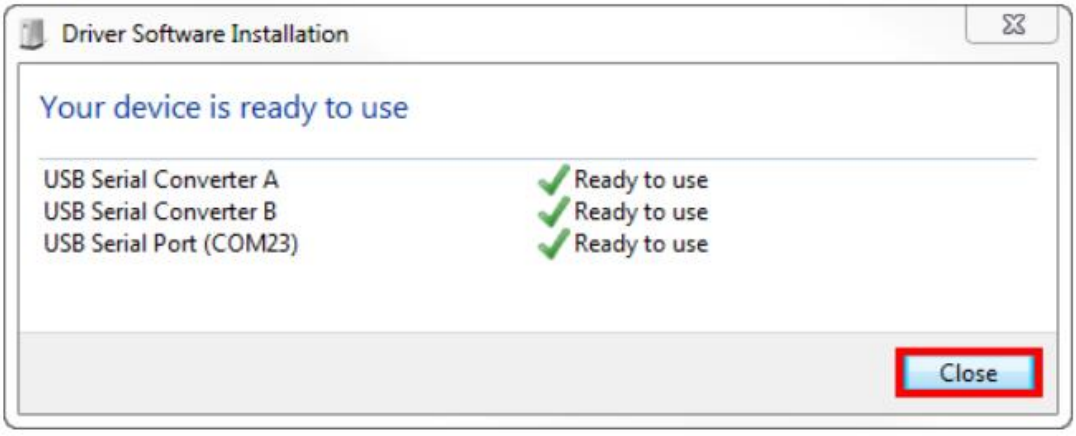


Part 3: Exporting the Design to the PLD Module

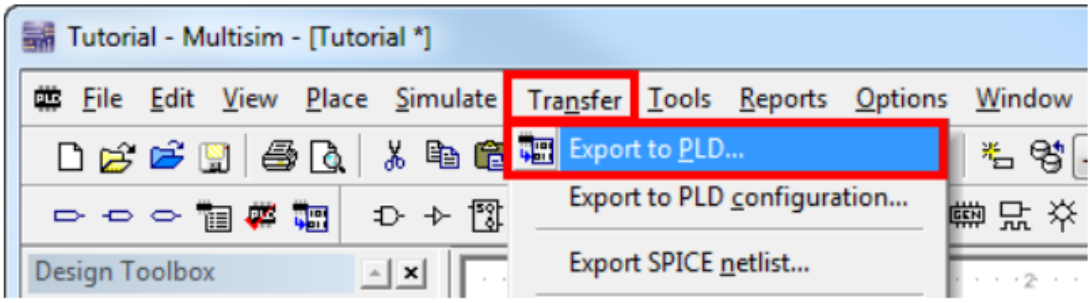
16 Install the PLD Module (PLTW S7) onto a breadboard so that the pins straddle the gap between pins.



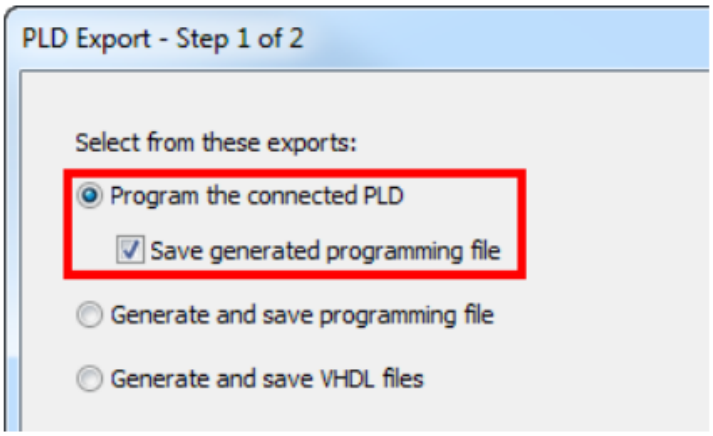
17 Connect the PLD Module to your computer using a USB micro cable. If this is the first time connecting the module then wait for the driver software installation process to complete. Select **Close**.



18 Select **Transfer** > **Export to PLD**.



19 On the Step 1 dialog screen leave the default option **Program the connected PLD** as export option > verify that the **Save generated programming file option** has a check mark > select **Next**.

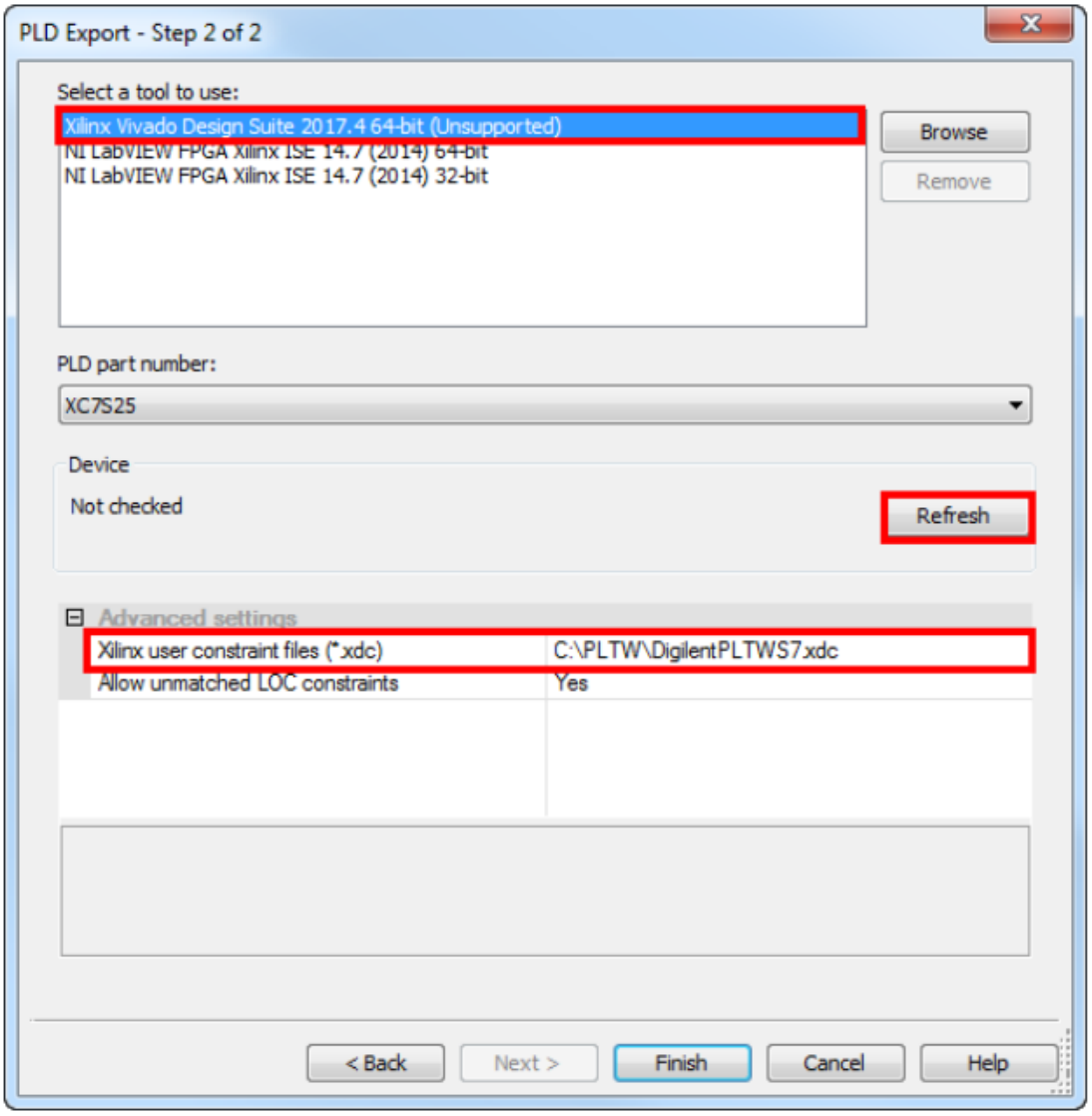


20 On the Step 2 dialog screen verify the communications with the board.

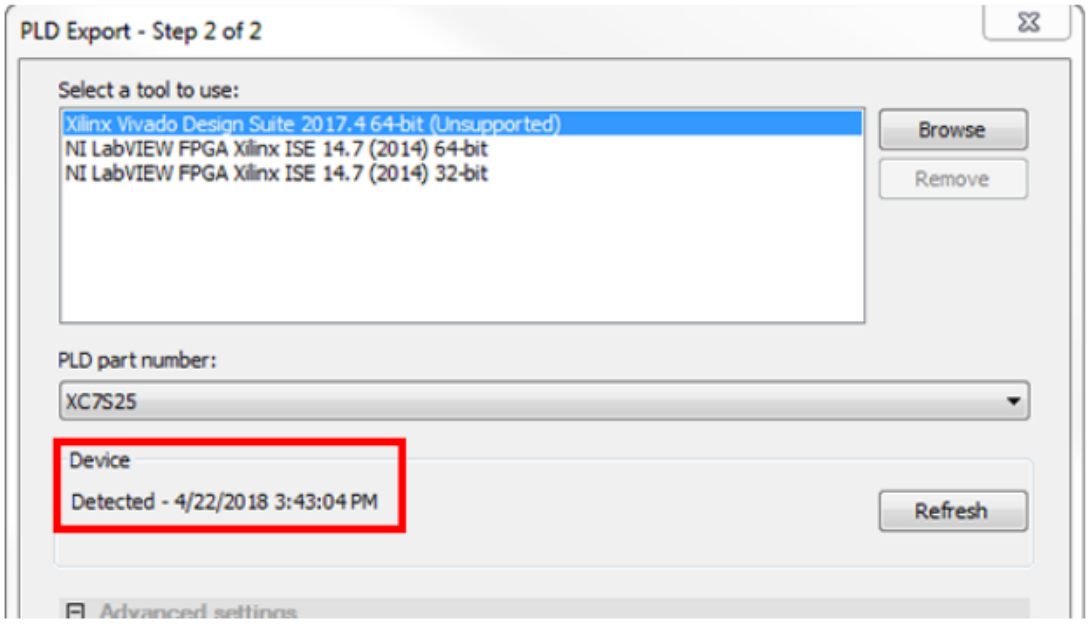
A. under Select Tool to Use select **Xilinx Vivado Design Suite 2017.4 64-bit (Unsupported)**.

B. Under the Advanced Settings section double click on **Xilinx user constraint files *(.xdc)*,** navigate to the folder where you copied the DigilentPLTWS7.xdc file e.g. C:\PLTW, and then select the file then **Open**. The Xilinx user constraint files (.xdc) field should display the file.

C. Select **Refresh**.



D. The Device Detected message should be displayed in the center of the dialog box indicating that the software is communicating with the PLTW S7.



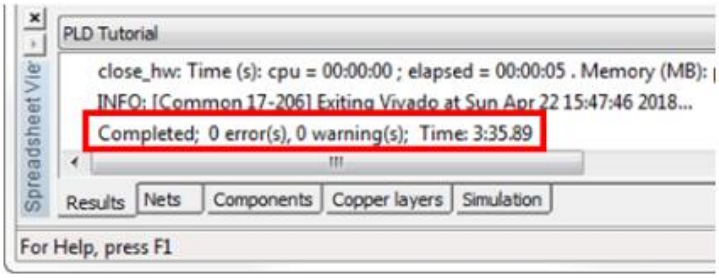
21 Select **Finish**. A sequence dialog boxes will show the progress of the four steps to export the program. Upon completion the status area will show the message of **Completed**. If the device is not found then verify that the common problems shown are not the problem. If you cannot solve the problem then tell your teacher so that steps can be taken to troubleshoot the problem.

a. Verify that the USB cable is properly connected.

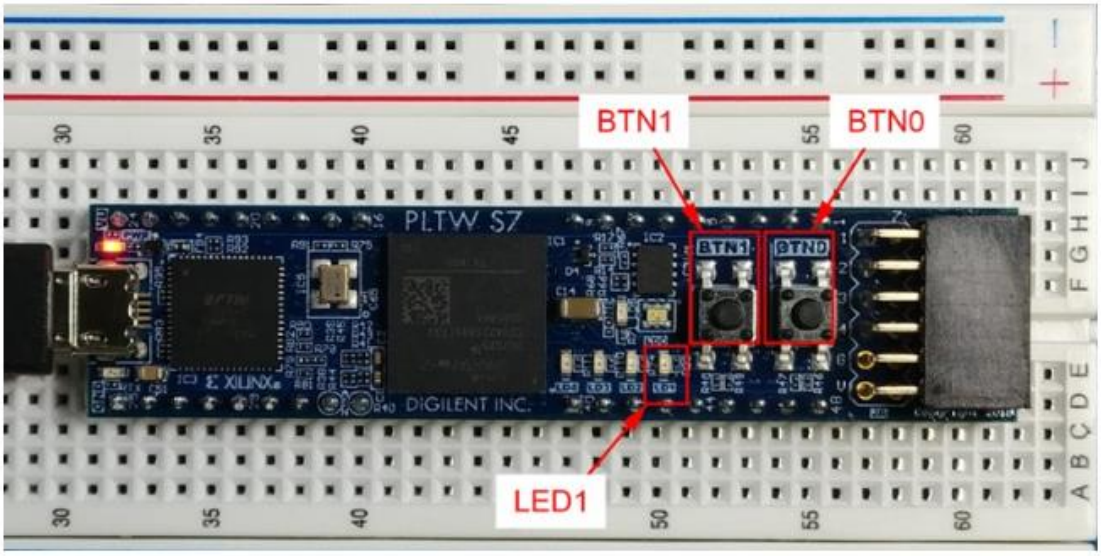
b. Verify that the Xilinx tools path was correctly set in Step 2.

c. Verify that the PLTW S7 was detected in the previous step.

Exporting to the PLD will take several minutes.



22 After the project is transferred then test the OR gate on the PLD so that it responds correctly. Refer to the **System Behavior video** for guidance.



CONCLUSION

1 Look up the names and definitions for the following programmable logic acronyms:

a. PLD:

b. PAL:

c. GAL:

d. CPLD:

e. FPGA:

2 The evolution of programmable logic devices from the simple PALs of the late 1970s to the FPGAs of today is a classic example of Moore's Law. What is Moore's Law?