PLD Design: Date of Birth Using PLTW S7

INTRODUCTION

Most designers would probably not prototype a design on a breadboard the way you did on the Date of Birth Problem. As the size and complexity of combinational logic circuits increase (or any circuits), their implementation with discrete logic gates becomes impractical. It requires many components and can take a long time to create and troubleshoot if not wired correctly.

To address this problem, the electronics industry has turned to programmable logic devices for designs of any complexity. The current state-of-the-art device for programmable logic is the **Field Programmable Gate Array (FPGA)**.

In this activity you will re-implement your Date of Birth design using the Field Programmable Gate Array (FPGA) on a **PLD**.

The original design specification from the Date of Birth Problem required that at least one of the segments be implemented in NAND logic and at least one of the segments be implemented in NOR. The reason for this requirement was to demonstrate the benefit in efficiency of NAND only and NOR only design implementations (fewer ICs as compared to AOI implementations).

With the FPGA implementation, this extra step of translating an AOI solution to a NAND (or NOR) solution is not necessary because the Xilinx Programming Software will automatically simplify the design into its most efficient implementation.

EQUIPMENT

These instructions are for use with the PLTW S7 shown. If you do not have the PLTW S7 then ask your teacher to guide you to the correct project.

Circuit Design Software (CDS)

- Digital MiniSystem (DMS):
  - myDAQ
  - myDigital Protoboard
  - PLTW S7 FPGA Module

- #22-gauge solid wire

- Combinational Logic Student Design Problem: Date of Birth

Procedure

Circuit Design in PLD Design Mode

1. Although the birthday design has already been created in Design Mode of the CDS, it must be recreated in the PLD Design Mode of the CDS.

   a. There are no design constraints on this PLD design. Using what you have learned, create your Date of Birth design in PLD Design Mode on the CDS.

   b. Use your engineering notebook and previous tutorials as a guide to recreate the circuit as simply and quickly as possible.

   c. There is not a seven-segment display option in PLD Design Mode that will let you simulate this circuit. You will need to test your design by programing the PLD and testing it on the breadboard.

Mapping PLD Pin Inputs/Outputs
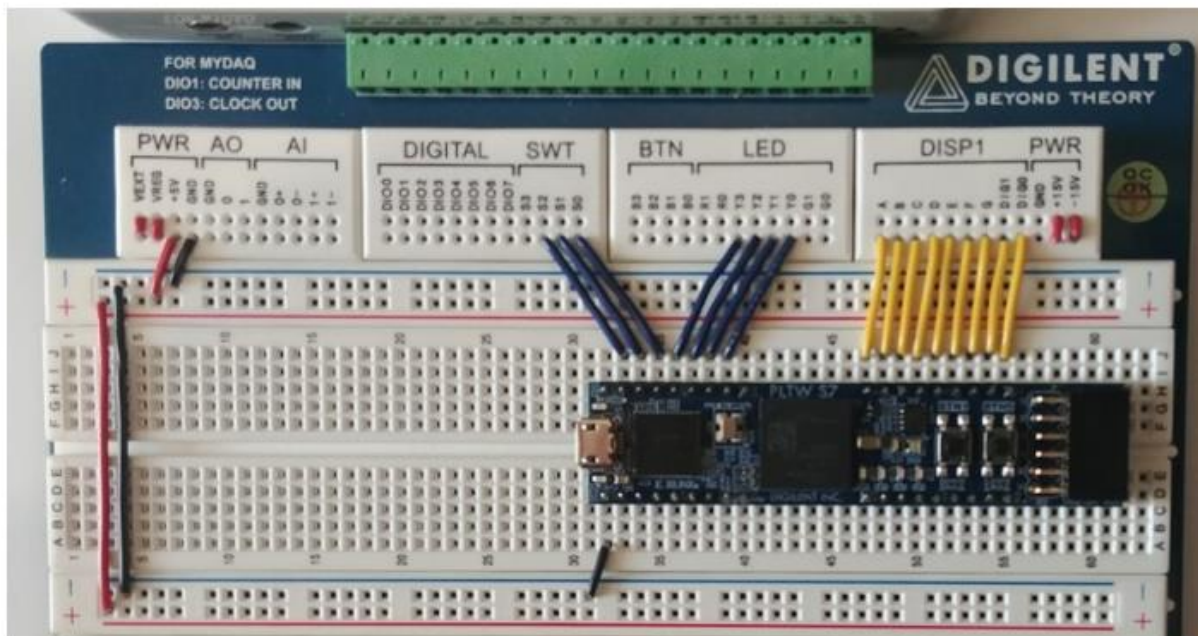
2. Map the design's three inputs (X, Y, and Z) to the pin inputs/outputs (PIOs) shown in the image.

PIO21_C X

PIO22_C Y

PIO23_C Z
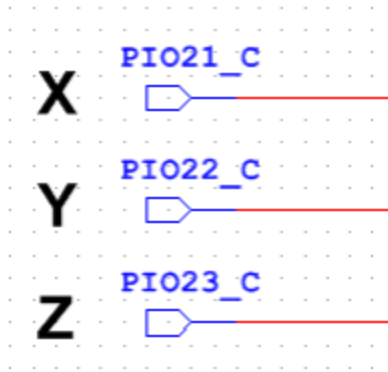
3. Connect the DMS slide switches SW2(X), SW1(Y), and SW0(Z) to the PIOs shown in the physical wiring image (SW0(Z) to PIO21, SW1(Y) to PIO22, and SW2(X) to PIO23).

4. The DMS has a Common Cathode SSD (0). To use DIG0, but not DIG1 then DIG0 must be connected to ground. Instead of physically placing a wire between DIG0 and GND it is more convenient to manage this in CDS.

U9 **DIG1_PIO02**

1

DIGITAL_HIGH

U10 **DIG0_PIO01**

0

DIGITAL_LOW
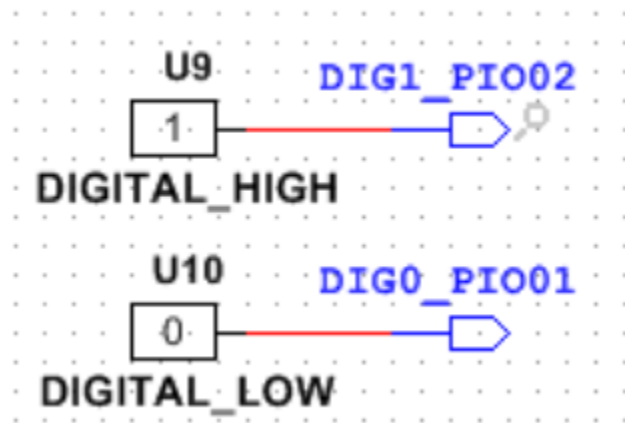
5. Connect PIO1 to DIG0 and PIO2 to DIG1. Refer to the physical wiring image.

6. Map the design's seven outputs (A, B, C, D, E, F, and G) to PIOs shown in the image.

SEGA_PIO09

SEGB_PIO08

SEGC_PIO07

SEGD_PIO06

SEGE_PIO05

SEGF_PIO04

SEGG_PIO03
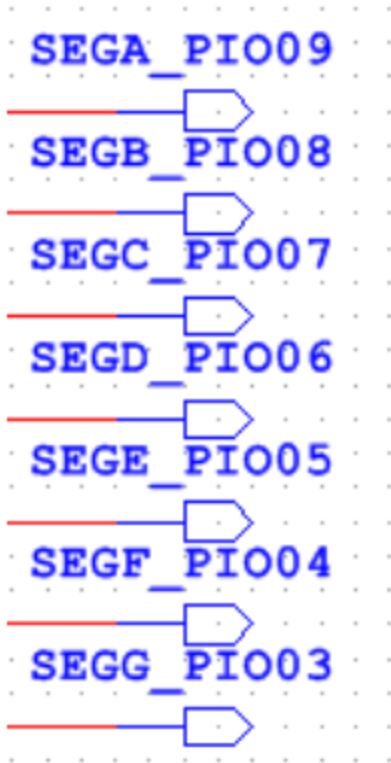
7. Connect the segments of the display labeled as DISP1A through DISPG to the PIOs shown in the physical wiring image (for example DISP1A to PIO9 and DISP1G to PIO3).

8. The wires between PIO17 through PIO20 to the LED inputs are not used in this activity.

9. Connect the remaining power and ground wires as shown in the physical wiring image.

10. Design then test your project by transferring to the PLTW S7.

CONCLUSION

1. Describe the strategy you used to recreate the Date of Birth design in PLD design mode? Did you take any shortcuts to create the circuit quickly?
2. List three advantages of implementing combinational logic design with programmable logic versus traditional discrete logic design.