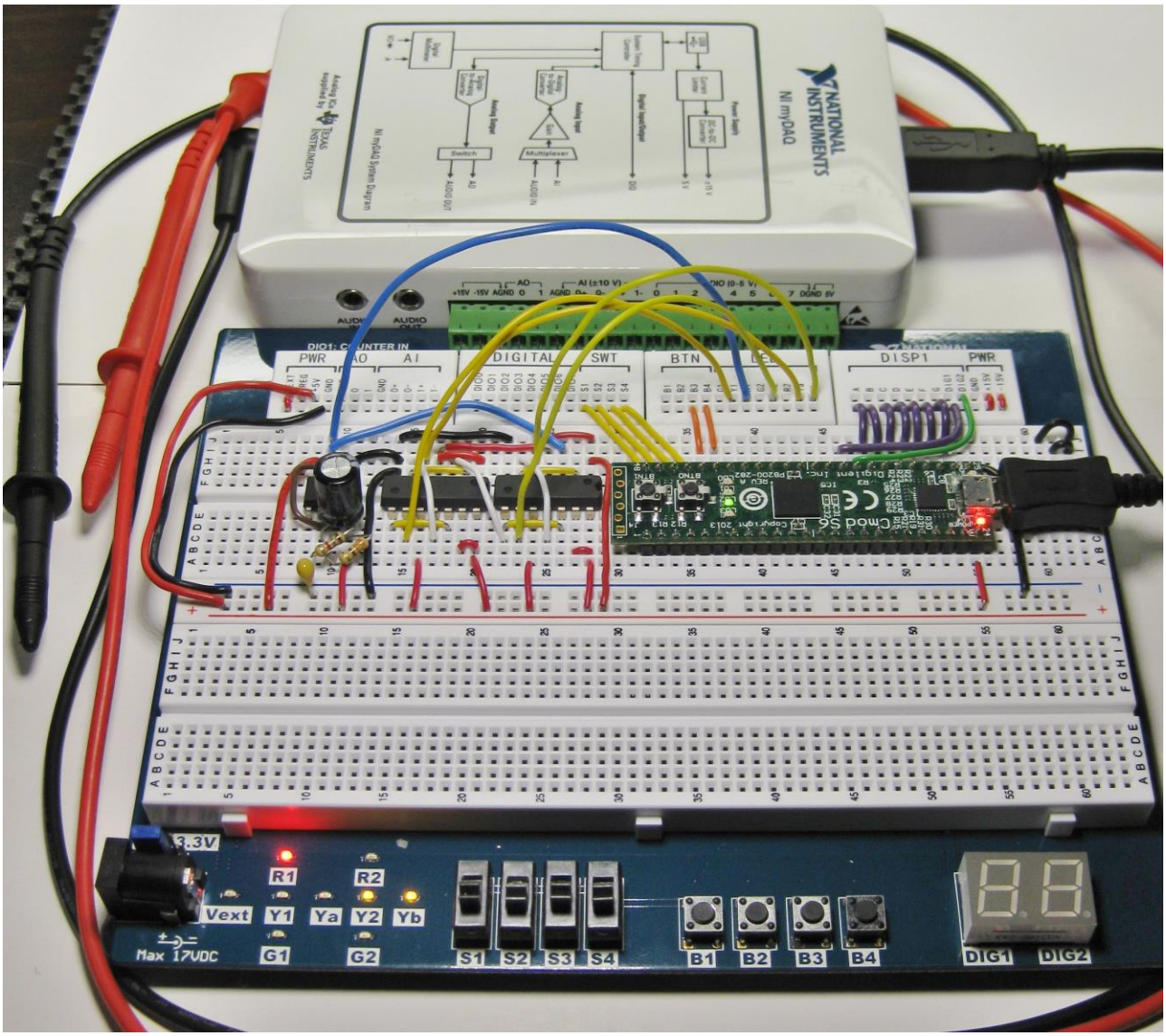
PLTW | Engineering

2014 Readiness and Core Training
Complete Start Guide: NI Digital MiniSystem (DMS)
myDAQ; myDigital Protoboard; Cmod S6 FPGA Module

Digilent Revision: August 13, 2013 Author: Marshall Wingerson
PLTW Revision: October 25, 2013 Author Jason Rausch

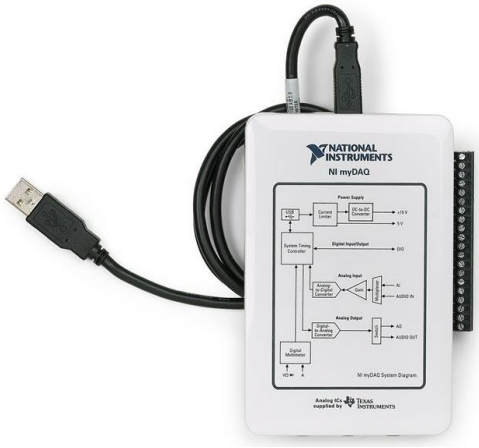


NI Digital MiniSystem (RevB)

This is a guide on how to start using the Digital MiniSystem. The Digital MiniSystem is made up of three development tools: myDAQ, myDigital Protoboard, and the Cmod S6 FPGA Module. These instructions support the installation of software for use of both Digital MiniSystem and the Digital Logic Board in the DE classroom.

NI myDAQ™

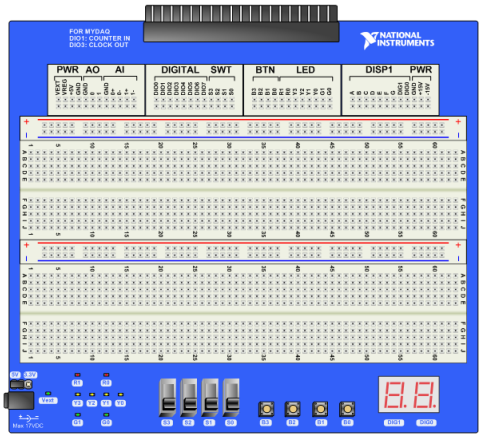
NI myDAQ is a Data Acquisition Module that features commonly used plug-and-play computer-based lab instruments based on LabVIEW including: a digital multimeter (DMM), oscilloscope (OSCOPE), and function generator (FGEN).



NI myDAQ™

NI myDigitialProtoboard™

The myDigital Protoboard is designed to work in conjunction with myDAQ to provide high school students with a cost-effective, portable, and engaging platform for teaching electronics. Along with NI Multisim, the myDigital Protoboard and myDAQ provide everything needed that will allow students to design, construct, and test basic analog and digital designs from combinational logic and sequential logic through simulation and prototyping.



NI myDigitialProtoboard™

Digilent Cmod S6™ FPGA

As the course progresses, circuits become larger and more complex. Students are introduced to programmable logic design using Multisim's PLD Mode. This allows students to program a powerful FPGA module that plugs into the same breadboard design area, replacing a large number of discrete ICs. The Cmod-S6 PLD Module provides the same programming experience as the current Digital Logic Board (DLB).

Digilent Cmod S6™ FPGA

Readiness Training:
Required Software Installation Overview:

The following is a list of the required software in the order it should be installed. It is critical that these specific installers be used and that the installation be done in exactly this order. Full versions of Xilinx downloaded from the Xilinx website will not allow the hardware to connect and you will experience licensing issues.

You must have full Administrator Rights on your laptop for the software and hardware to function properly at Core Training.

Note: Xilinx does not currently support Windows 8 (Windows 7 and Windows 8.1 will work).

- **Multisim 12.0.1**
- **NI LabVIEW FPGA Xilinx 12.4 SP1 Tools**
- **LabVIEW 2013 FPGA Module Xilinx Tools 14.4**
- **DEFB Driver (For use of DLB. Not required in Core Training. Required school install.)**
- **digilent.cseplugin_v2.6.3**
- **NI ELVISmx 4.4 Driver**

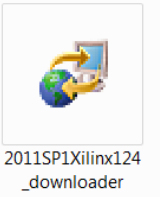
Multisim 12.0.1 – Installation Instructions

1. Within the LMS navigate to the **Software Installation** module.
   a. Select the "***Install – Multisim12.0.1***" assignment.
   b. There you will find: "***Installation Guide: Circuit Design Suite – Multisim 12.0.1***"
   c. Install Multisim 12.0.1 according to the installation guide.

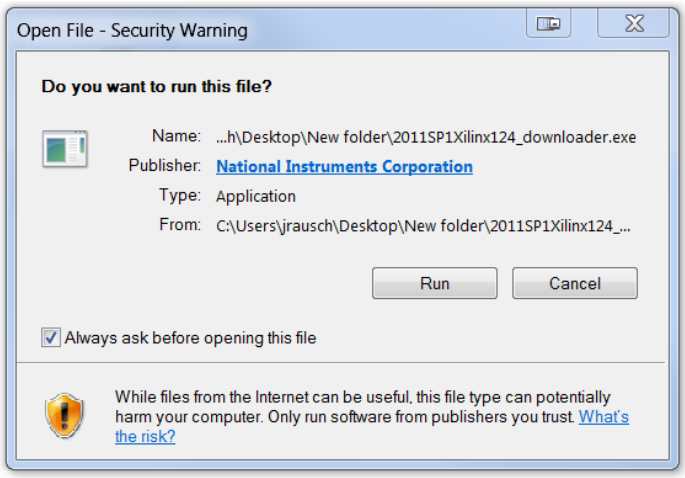
Xilinx 12.4 – Installation Instructions

The following instructions describe the installation process for Xilinx 12.4

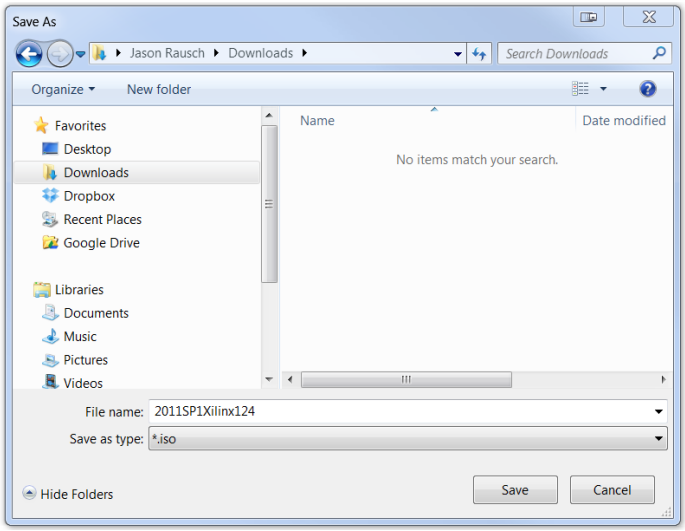
2. Click here to install **"NI LabVIEW FPGA Xilinx 12.4 SP1 Tools".** This will provide you with the NI Downloader executable from the NI website. This installer can also be found within the DE Core Training LMS course module under "Software Installation".

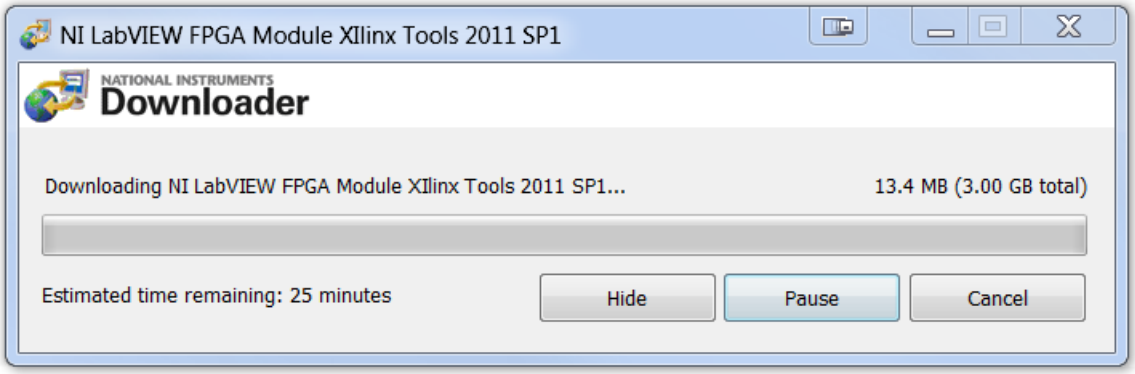


3. Run “**2011SP1Xilinx124_downloader**”. When you run the downloader it will ask you to save the downloader as an iso file.



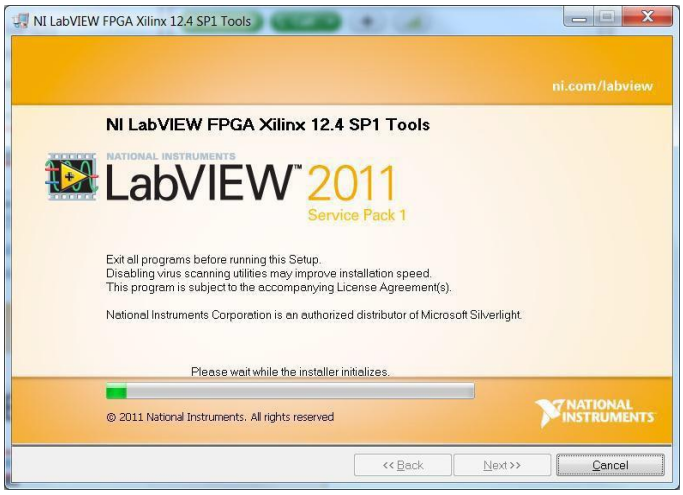
4. Choose an appropriate location to save the “2011SP1Xilinx124” iso file and download.





5. **Unzip** “2011SP1Xilinx124” with a program such as **WinZip**.
    a. Select: “**Install NI LabVIEW FPGA Xilinx 12.4 SP1 Tools**”.

6. Installation Process: “**NI LabVIEW FPGA Xilinx 12.4 SP1 Tools**”

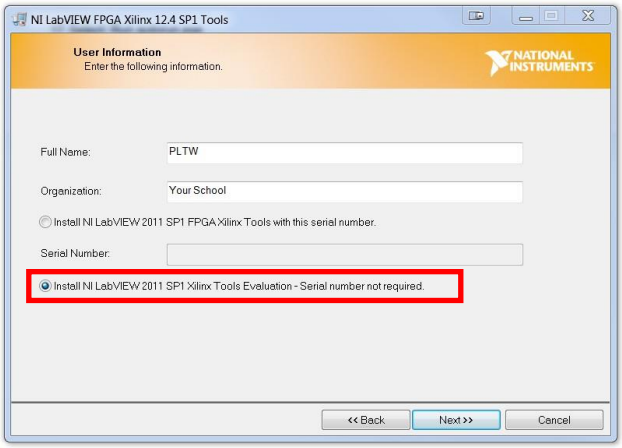


7. After installation of “**NI LabVIEW FPGA 12.4 SP1 Tools**”
    a. Select: **Next**

8. **Fill out the following fields**:

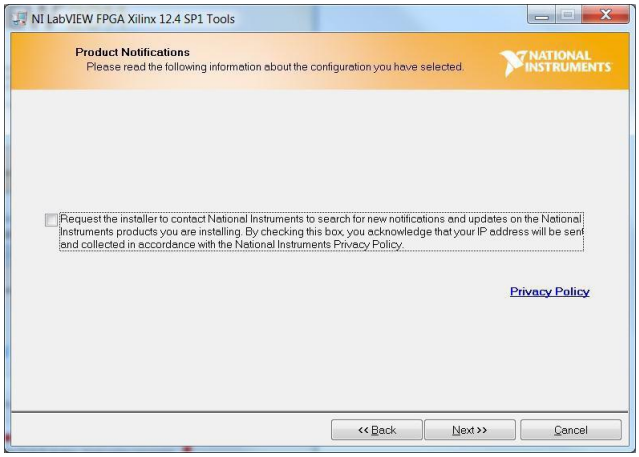
   Full Name:
   Organization:
   Select:

   "Install LabVIEW 2011SP1 Xilinx Tools Evaluation – Serial number not required"



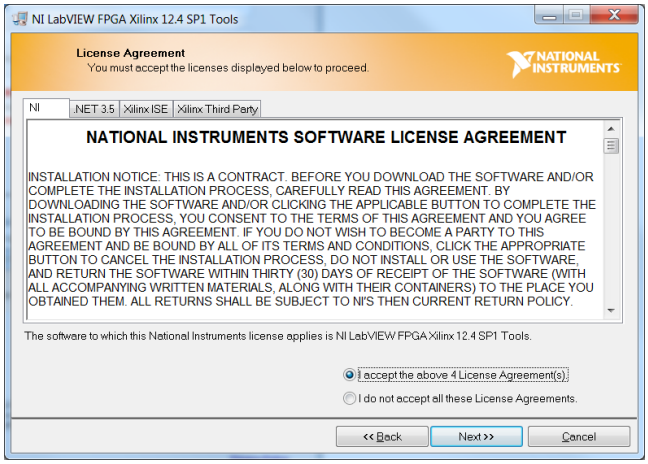
9. **Uncheck box** to contact NI and search for updates. You will update *after* the install and activation of "**NI LabVIEW FPGA 12.4 SP1 Tools**".

   a. Select: **Next**

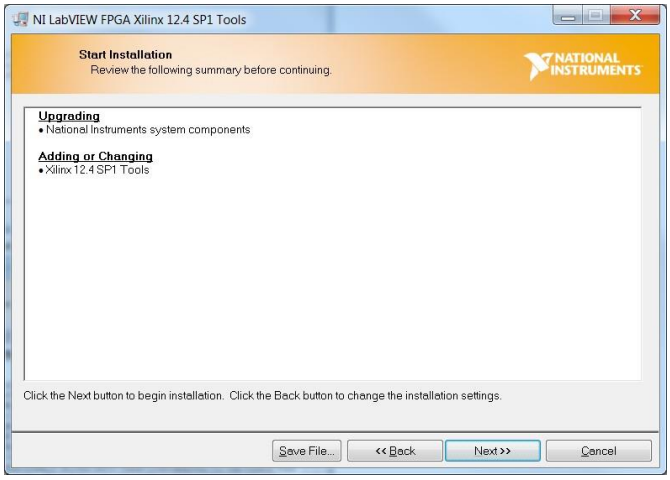


10. Select: **I accept the above 4 License Agreements.**

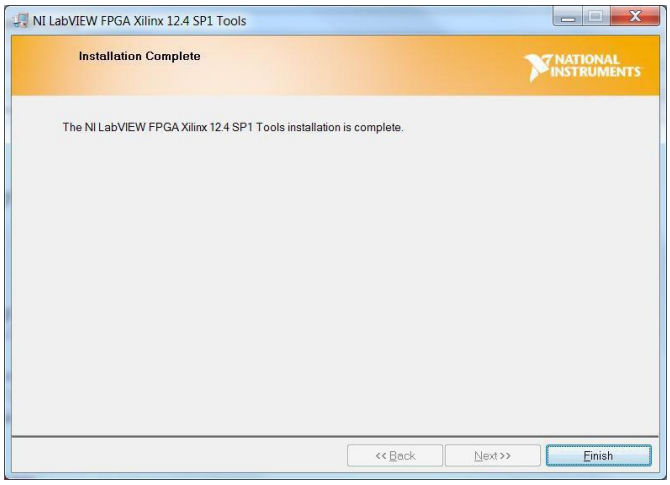
    a. Select: **Next**



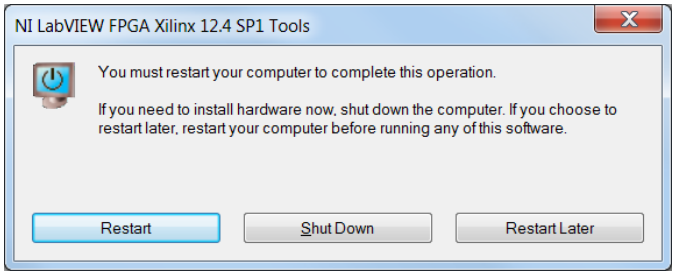
11. Select: **Next**



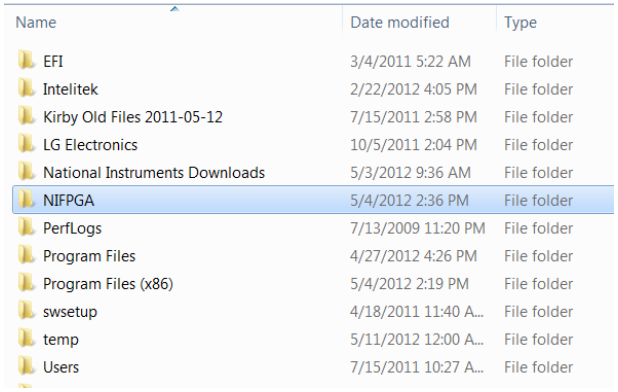
12. Select: **Finish**



13. You will need to restart your computer.



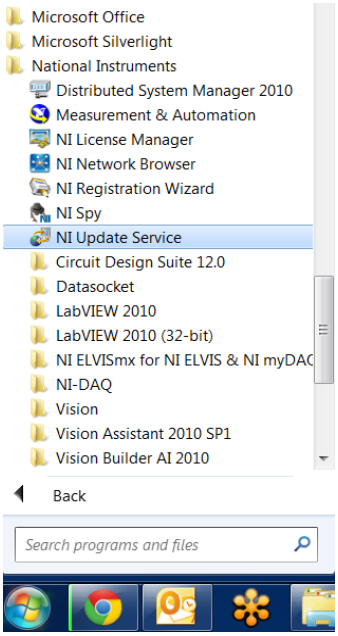
14. "**Xilinx 12_4**" is now located in the following folder location "**C:NIFPGA**".



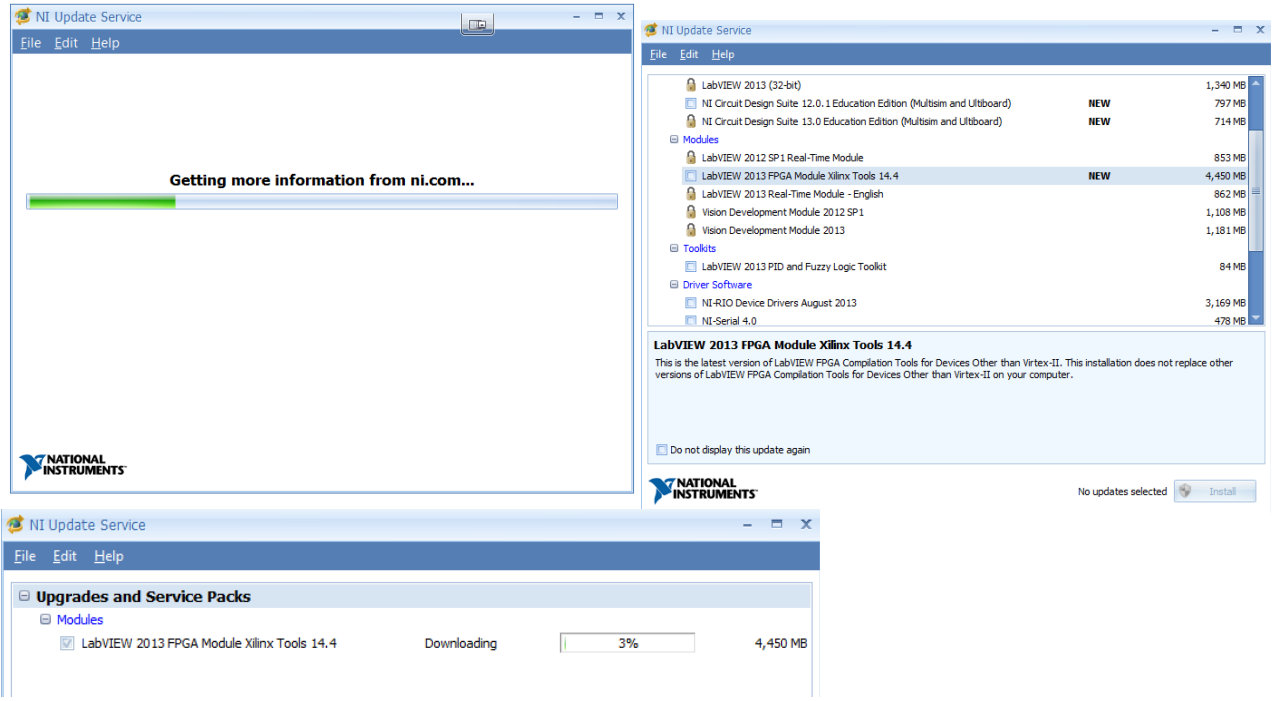
Xilinx 14.4 Update Instructions

15. To add the update "**LabVIEW 2013 FPGA Module Xilinx Tools 14.4**":

    Open: **NI Update Service**
    Navigate to: **"Start" -> "All Programs" -> "National Instruments"**
    Select: "**NI Update Service**"



16. Select: "**LabVIEW 2013 FPGA Module Xilinx Tools 14.4**"
    Select: **Install**



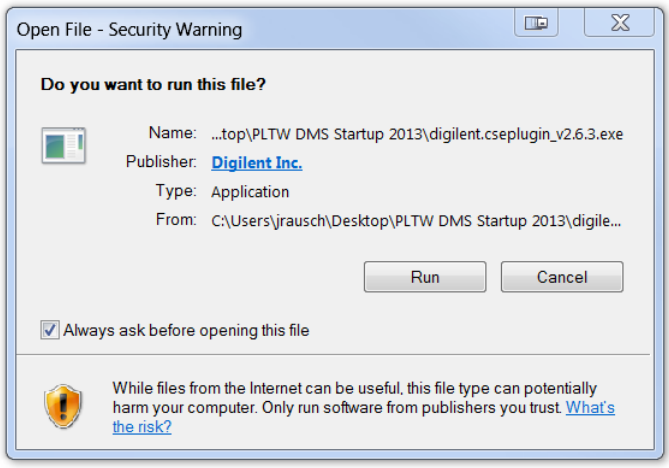
16. Some schools might block the NI Update Service. You can download and install directly from NI here if you are unable to use the NI Update Service at your location:
    LabVIEW 2013 FPGA Module Xilinx Tools 14.4

Digilent.cseplugin_v2.6.3 – Installation Instructions

The following instructions describe the process to download (2) driver files needed to operate the Cmod S6 FPGA Module with Multisim, Xilinx, and your computer. The **Digilent plugin_v2.6.3** will provide you with the correct .cse file and install Adept, giving you access to the Cmod S6 driver.

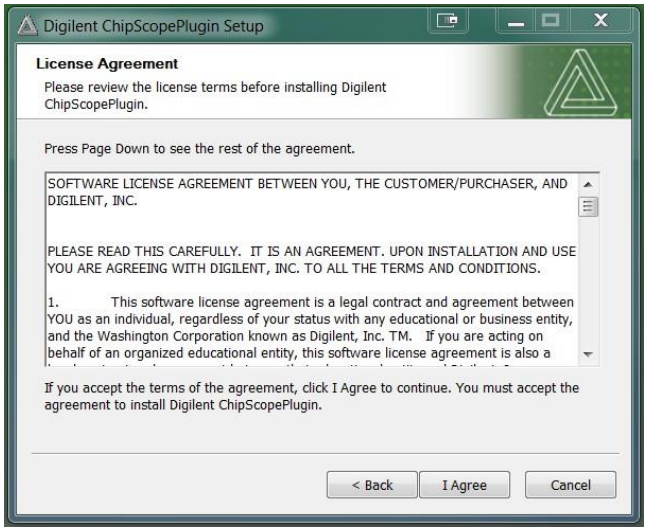
17. Within the LMS navigate to the **Software Installation** module.
    a. Select the "***Software Installation Guide: Digital MiniSystem (DMS)".***
    b. There you will find "***Digilent.cseplugin_v2.6.3***" under 2014-2015 Software installation.
       Note: CT Instructors can download from the VA here: **Digilent.cseplugin_v2.6.3**
    c. Download "***Digilent.cseplugin_v2.6.3***".

18. Select: **Run**

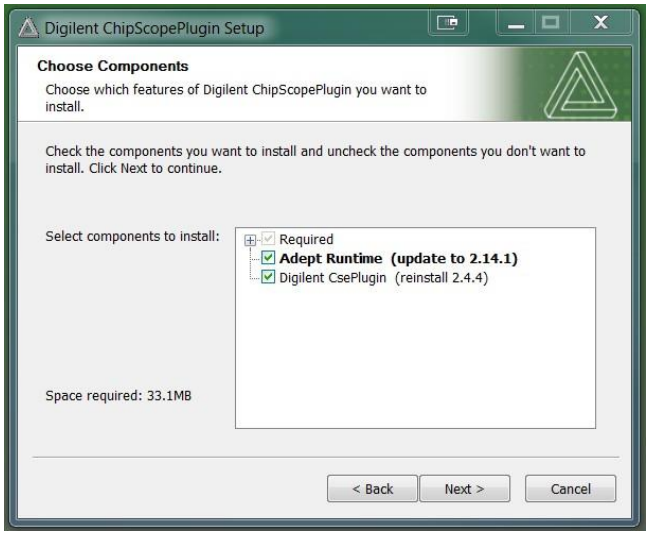


19. Select: **Next**

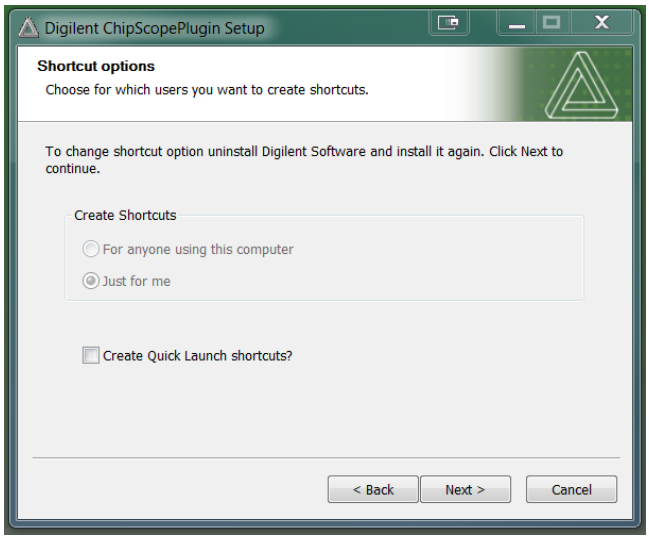
20. Select: **I Agree**



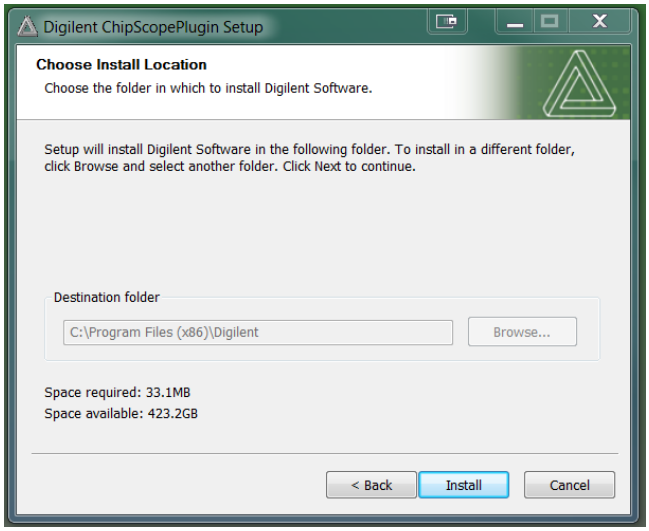
21. Check Boxes: "**Adept Runtime**" and "**Digilent CsePlugin**"
    a. Select: **Next**



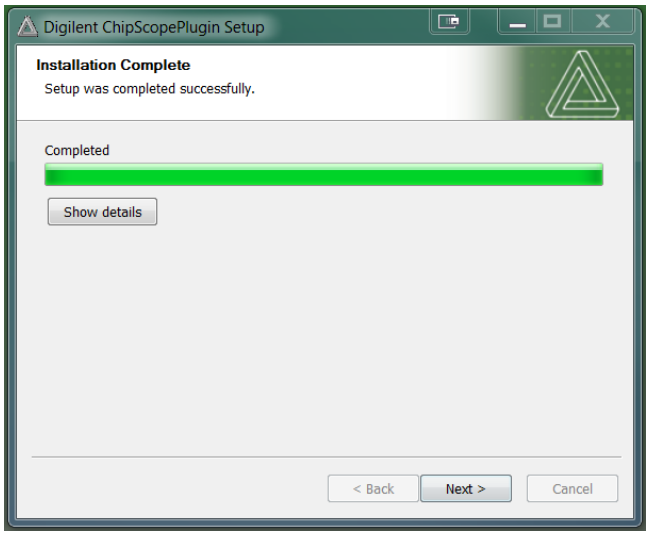
22. Uncheck Box: **Create Quick Launch Shortcuts**



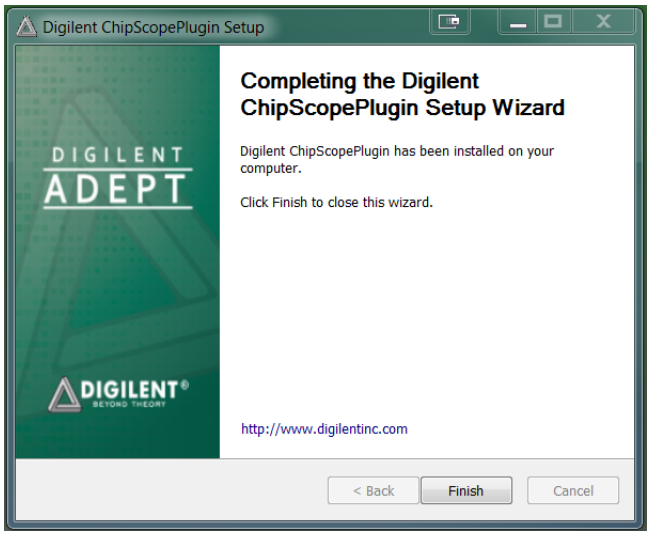
23. Select: **Install**



24. Select: **Next**



25. Select: **Finish**



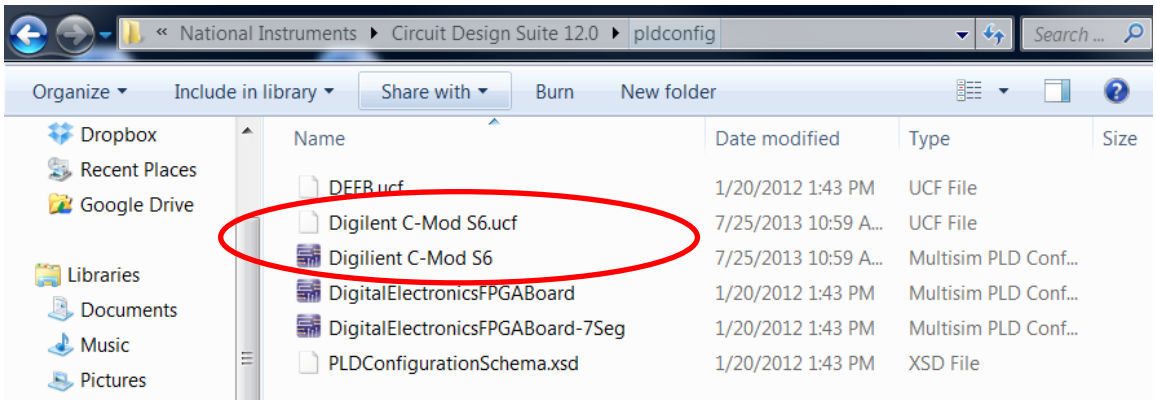
Adding Multisim Configuration and User Constraint Files

26. Within the LMS navigate to the **Software Installation** module.
    a. Select the "***Software Installation Guide: Digital MiniSystem (DMS)"***
    b. Under "***Configuration and User Constraint Files***". There you will find two files that must be placed within the pldconfig folder.
        - "Digilent C-Mod S6.mspc"
        - "Digilent C-Mod S6.ucf"
    c. Download the two files from the LMS. Note: CT Instructors can download from the VA here **Digital MiniSystem Configuration Files**.

27. Navigate to:

    C:\Program Files(x86)\National Instruments\Circuit Design Suite 12.0\pldconfig

28. Copy the two (2) files to the pldconfig folder.



NI ELVISmx 4.4 – Installation Instructions (Optional)

The following instructions describe the process to download the driver required to use the myDAQ. This installation is optional for readiness training. The driver can be loaded directly from the CD upon arrival at your Core Training site.

29. Within the LMS navigate to the **Software Installation** module.
    a. Select the "***Software Installation Guide: Digital MiniSystem (DMS)".***
    b. Under "***Software Installation***" you will find the "**NI ELVISmx 4.4 Downloader Tool**" .
    c. Select the "**NI ELVISmx 4.4 Downloader Tool**" and install the NI ELVIVmx 4.4 Driver for use with the NI myDAQ.

30. You now have all necessary software, drivers, and files to use the Digital MiniSystem.

Getting Started at Core Training:
Testing Configuration of the Digital MiniSystem

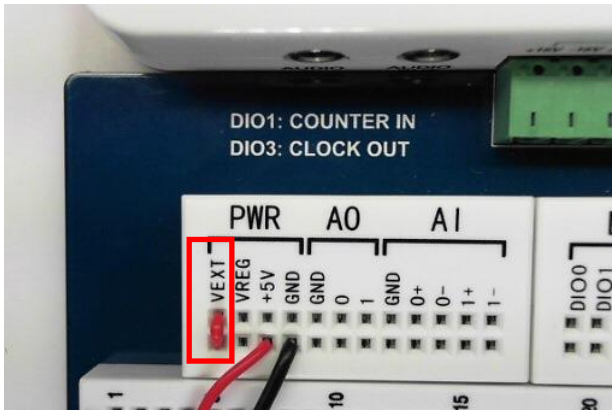
Required Hardware:

- Computer with Software Installed
- National Instruments myDAQ with USB
- National Instruments myDigital Protoboard
- Cmod S6 FPGA Module
- Micro-USB B Cable
- 22 Gauge Solid Wire

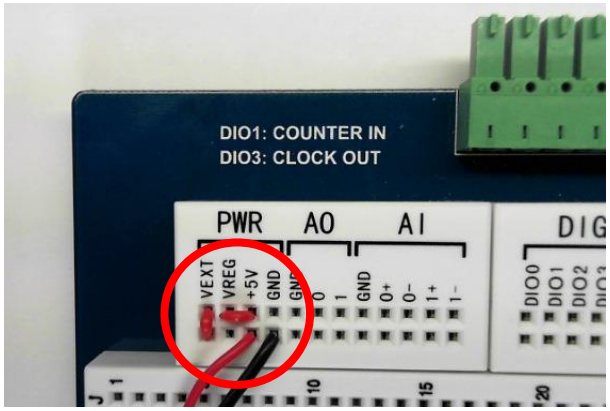
Powering the myDigital Protoboard

There are two options for powering the MyDigital Protoboard.

31. **myDAQ as power source** – With the MyDigital Protoboard coupled to the myDAQ +5V is supplied from the +5V PWR located at the top left of the board.
32. **VEXT as power source (**17V Max external battery or AC/DC adaptor) – When not tethered to the myDAQ, the MyDigital Protoboard can be powered by jumping from **VREG to +5V PWR** located at the top left of the board. The VEXT is a standard coaxial power connector (5.5mm X 2.1mm) commonly available on DC wall adapters (max 17VDC).

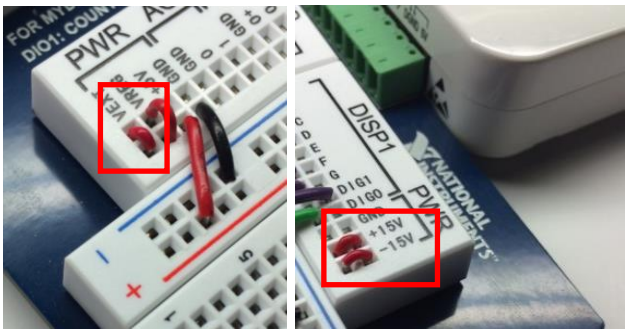


Powered by myDAQ



Powered by External Voltage (17VMax)

It is highly recommend that VEXT, +15V, -15V be blocked off with a loop of wire (as shown) so that students do not exceed 5V on the CMOD S6 PLD Module.



DO NOT WIRE VEXT, +15V, -15V TO THE PLD MODULE. The CMODS6 will fail above 5V.

Powering the Cmod S6 FPGA

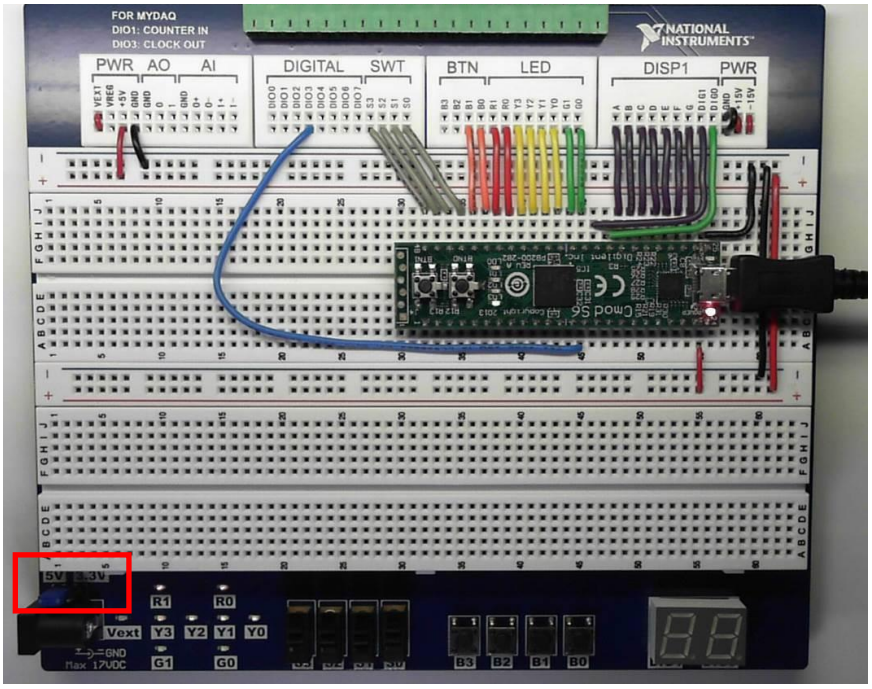
33. **Micro-USB B cable to power the PLD Module** – The Cmod S6 FPGA Module can be powered with the module tethered to a computer alone. However, the myDigital Protoboard must still be powered from Option #1 (myDAQ) or Option #2 (VEXT) if you wish to use the buttons or switches. The seven-segment display will also appear dim as they are not being powered by 5V.

Wiring the Digital MiniSystem

34. Connect the myDigital Protoboard to the myDAQ. With the Cmod S6 FPGA Module on your myDigital Protoboard, connect the Cmod S6 FPGA Module to your computer with the Micro-USB B cable. Let the computer install the required drivers for Cmod S6 FPGA Module use.
35. The myDigital Protoboard has a 5V or 3.3V option for TTL or CMOS (lower left corner). Confirm the jumper is set to 5V.
36. Connect a wire from +5V to the positive rail of the myDigital Protoboard.
37. Connect a wire from GND to the negative rail of the myDigital Protoboard.
38. Connect a wire from the positive rail to pin number 24 of the Cmod S6.
39. Connect a wire from the negative rail to pin number 25 of the Cmod S6.
40. Now that the board has external power from the myDAQ, remove the USB port and check that the red LED on the Cmod S6 is still lit.
41. All answer keys and PLD Mode simulations related to the Digital MiniSystem will use these assigned pins. The myDigital Protoboard has been wired to be powered from the myDAQ.

Cmod – myDigital Protoboard

PIO14 – DIO3 (CLK from myDAQ)
PIO24 – VCC
PIO25 – GND
PIO26 – G
PIO27 – F
PIO28 – E
PIO29 – D
PIO30 – C
PIO31 – B
PIO32 – A
PIO33 – DIG 0
PIO34 – DIG 1
PIO35 – G0
PIO36 – G1
PIO37 – Y0
PIO38 – Y1
PIO39 – Y2
PIO40 – Y3
PIO41 – R0
PIO42 – R1
PIO43 – B0
PIO44 – B1
PIO45 – S0
PIO46 – S1
PIO47 – S2
PIO48 – S3



myDigital Protoboard with Cmod S6 FPGA Module

Cmod S6 FPGA Module - Factory Loaded User Demo

The Quad SPI Flash is loaded with a configuration file at the factory. When powered on, the file will configure the FPGA such that the buttons control the states of two LEDs, while the other two LEDs toggle at a speed of about 1 Hz. The general purpose I/O pins are initially configured as inputs, and are pulled up internally by the FPGA to read a logic level '1'.

Cmod S6 FPGA Module - Clocks

There are two clocks available on the Cmod S6 FPGA. There is an 8 MHz clock, and there is a 1 Hz clock. PIO14 is designated as a CLK input. See the Cmod S6 Reference Manual for more details.

Cmod S6 FPGA Module Test Files

The following three PLD Mode test files can be downloaded and unzipped to test the Cmod S6 FPGA Module.

42. Within the LMS navigate to the **Software Installation** module.
    a. Select the "***Software Installation Guide: Digital MiniSystem (DMS)".***
    b. There you will find the three (3) test files Multisim PLD Mode Test Files.
       Note: CT Instructors can download from the VA here **PLD Mode Test Files.**
    c. Download each file.

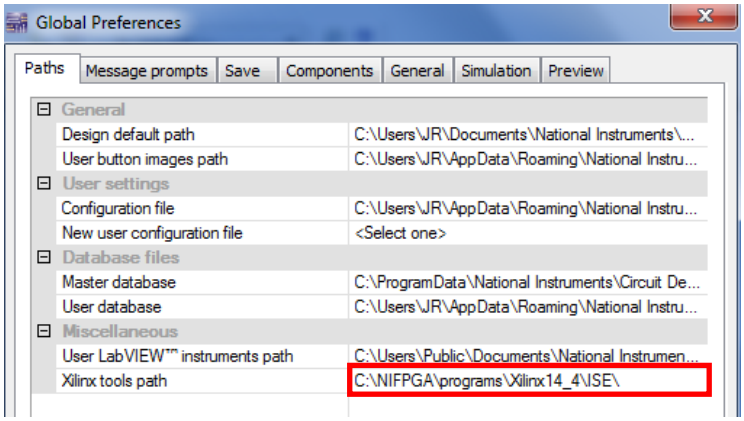
- **Internal Clock Test (DMS_14.4).ms12** – Demos how to integrate the internal clock signal of the PLD Module (Cmod S6). This test displays a 4 bit up count.
- **External Clock Test (DMS_14.4).ms12** – Demos how to use an external clock signal (myDAQ: Digital Writer Out). This test displays a 4-bit up count.
- **Multiplexed Display Test (DMS_14.4).ms12** – Demos full functionality of the Digital MiniSystem (DMS) based on the test set up configuration. This test displays a sixty second timer.

Export to PLD: Transferring a File to the Cmod S6 FPGA Module

43. Connect the Cmod S6 FPGA Module to your computer if with the USB cable if not already connected.
44. Open "Internal Clock Test" in Multisim.

45. Once the selected test file is open:

    Select: **Options -> Global preferences -> Paths -> Miscellaneous -> Xilinx tool path.**
    (Three dot box to the right side of the box)
    Make sure the **Xilinx tool path** is set to **C:\NIFPGA\programs\Xilinx14_4\ISE**



46. Select: **Transfer -> Export to PLD.** This will bring up a menu.

47. Xilinx tool:

- Under the Xilinx tool dropdown menu select:

  "Xilinx ISE Design Suite 14.4 32-Bit or Xilinx ISE Design Suite 14.4 64-Bit"
  Disregard (Unsupported) message if present.

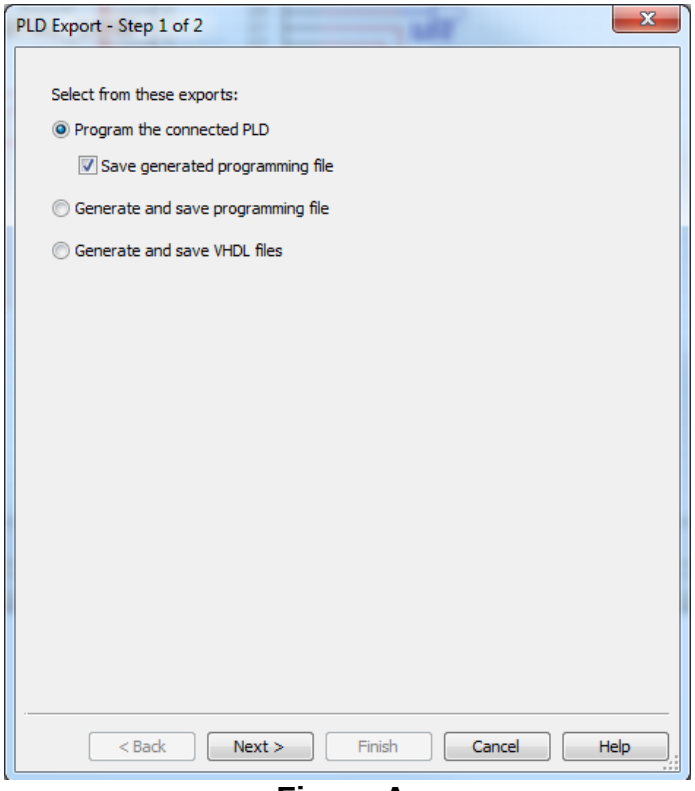


Figure A

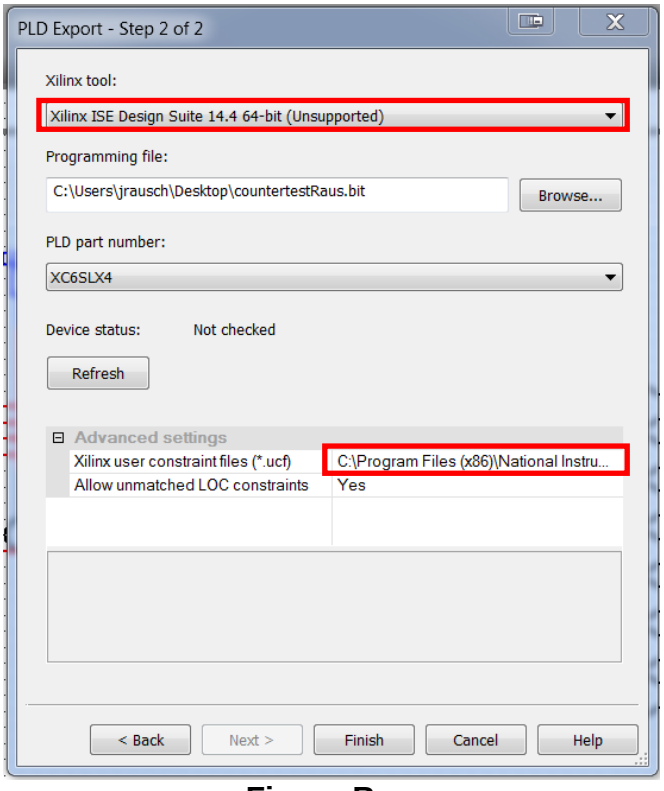


Figure B

Programming file: Select Browse: Set your location for the programming file if you are not already there.

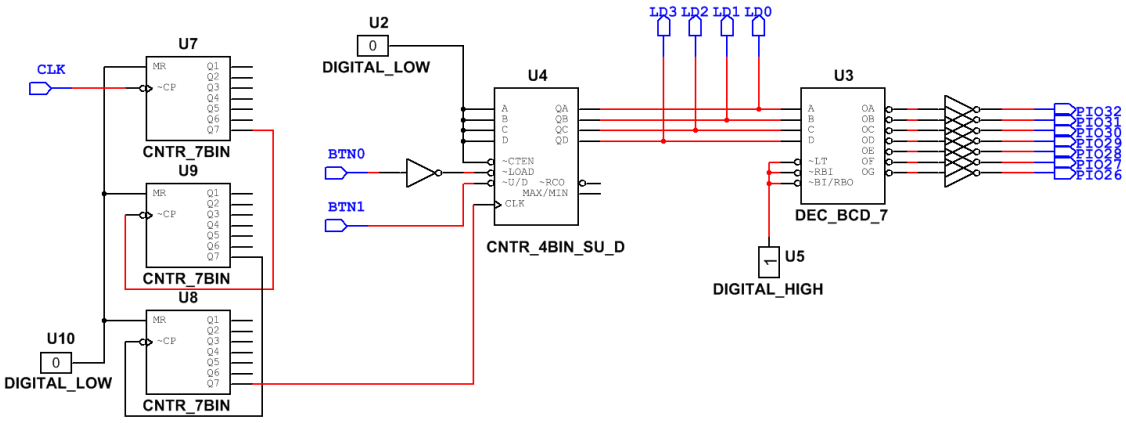
PLD part number: The PLD part number will auto-populate.

Advance settings: Under the advanced settings click the button on the right side of the Xilinx user constraint files row and select “Digilent C-mod S6.ufc” from pldconfig folder.

Xilinx user constraint files (*.ufc): Set path to **C:\Program Files\National Instruments\Circuit Design Suite 12.0\pldconfig**

Allow unmatched LOC constraints: Yes.

48. Select: **Finish**
49. Exporting to the PLD will take several minutes. If the device is not found:
    a. Check that the USB cable is connected.
    b. Check user constraint path under PLD export Step 2.
    c. Check the Xilinx tool path under Global Settings.
    d. Check your Device Manager to see if “Digilent USB Device” is found.
45. The PLD Mode simulation should be loaded on the Cmod S6 FPGA. All four green LEDs should be displaying a new pattern (not Demo Mode).
46. This demo “Internal Clock Test (DMS_14.4**)”** will display a 4-bit binary up count on the green LEDs of the Cmod S6 FPGA Module, and a numerical count on the seven-segment display.
    Note: The seven-segment display will show the SSD equivalent of the numbers 10-15.

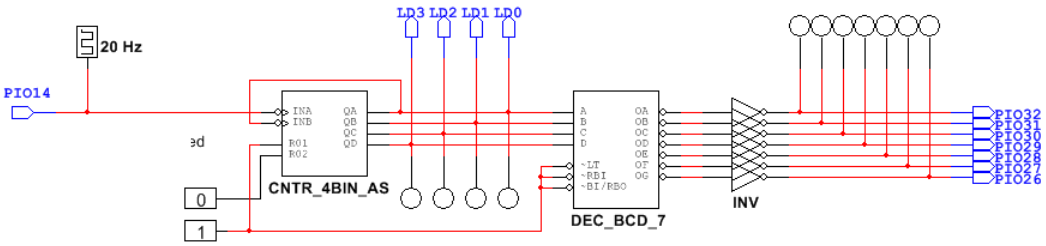


Circuit Design in Multisim PLD Mode

Using a myDAQ Clock Signal: External Clock Test (DMS_14.4)

This demo will display a 4-bit binary up count on LEDs of the Cmod S6 FPGA Module, and a numerical count on the seven-segment display. The clock signal will be generated using the NI Elvis Digital Writer on the myDAQ.

The myDigital Protoboard should be powered by the myDAQ. Wire DIG0 to GND for this demo as it was in the first demo.



Circuit Design in Multisim PLD Mode

47. From the downloaded and unzipped folder:

    Open: **"External Clock Test (DMS_14.4)"**

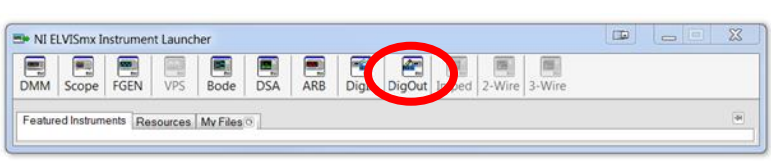
48. Export to PLD: Transfer the file to the Cmod S6 FPGA as you did with the previous test file.

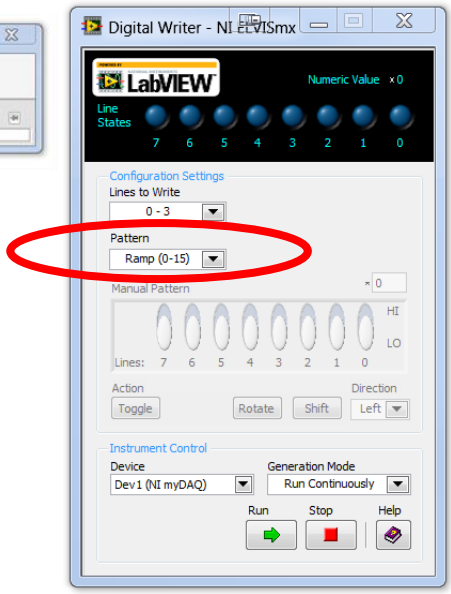
49. Wire **DIO3** from the myDigital Protoboard to **PIO14** of the Cmod S6 FPGA.

50. Navigate to:

    Program -> National Instruments -> NI ELVISmx for NI myDAQ ->
    NI ELVISmx Instrument Launcher

51. Open the NI Elvis Digital Writer (DigOut) on the myDAQ to generate a clock signal.
    Select: (Write lines 0-3 Ramp 0-15)





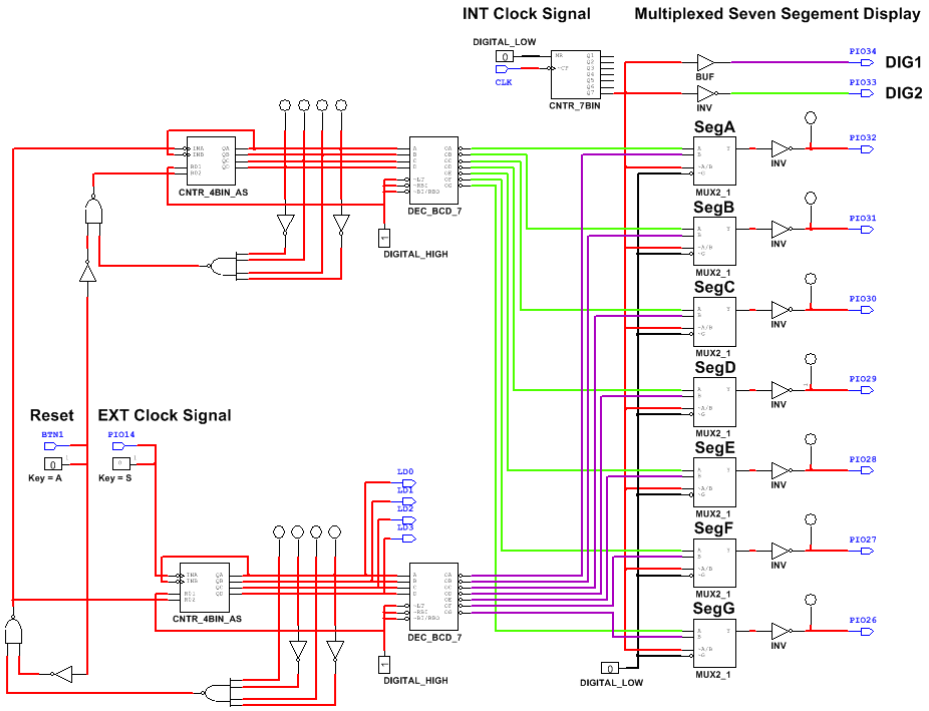
52. To adjust the frequency of the clock, move the wire from DIO3 to DIO2 and so on to speed up the clock signal.

Using the Multiplexed Display: Sixty Second Timer (DMS_14.4)

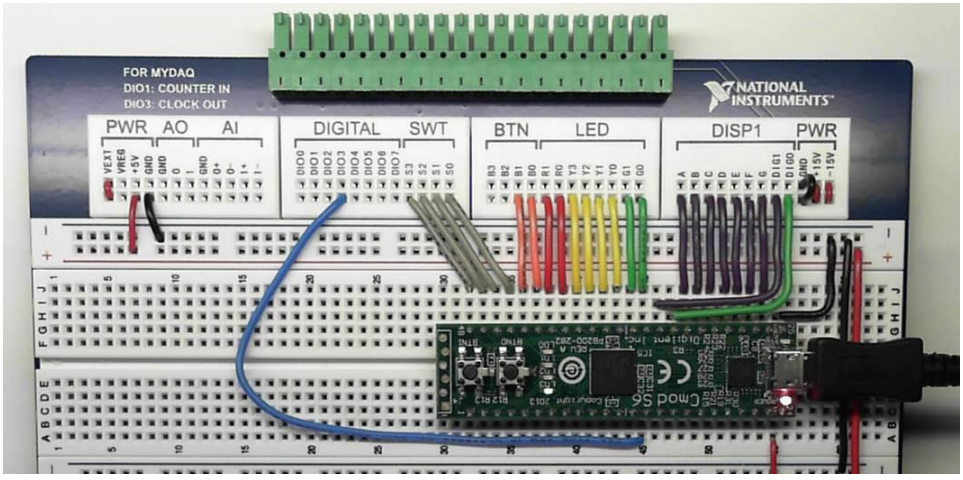
This demo will display a count from 0-60 on the multiplexed seven-segment displays. The internal clock of the Cmod S6 multiplexes the SSD so that 2 digits can be shown.

The switches (S0-S3) and buttons (B3 and B4) can be tested with outputs to RED, GREEN, and YELLOW LEDs. The myDigital Protoboard should be powered by the myDAQ.

Note: If using a student version of Multisim, you may get an error message related to the number of components in the file.



Multiplexed Circuit Design in Multisim PLD Mode



Wiring for myDigital Protoboard and the Cmod S6 FPGA

53. From the downloaded and unzipped folder:

    Open: **“Sixty Second Timer (DMS_14.4)”**

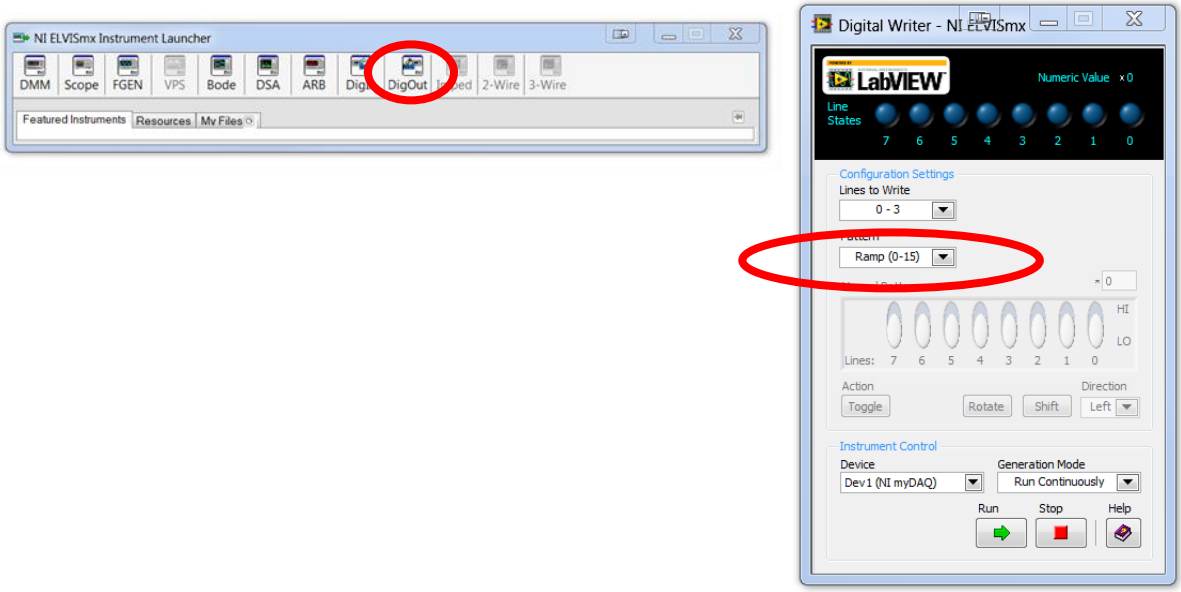
54. Export to PLD: Transfer the file to the Cmod S6 FPGA as you did with the previous test file.

55. **DIO3** from the myDigital Protoboard should be wired to **PIO14** of the Cmod S6 FPGA.

56. Navigate to:

    Program -> National Instruments -> NI ELVISmx for NI myDAQ ->
    NI ELVISmx Instrument Launcher

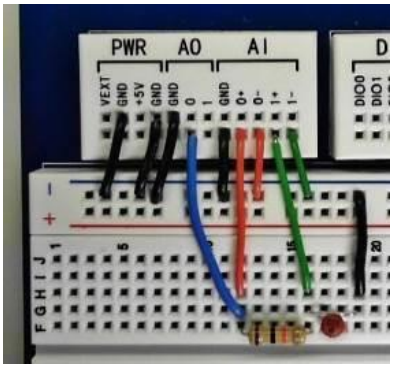
57. Open the NI Elvis Digital Writer (DigOut) on the myDAQ to generate a clock signal.
    Select: (Write lines 0-3 Ramp 0-15)



58. To adjust the frequency of the clock, move the wire from DIO3 to DIO2 and so on to speed up the clock signal.

Using myDAQ Instrumentation with the Digital Minisystem

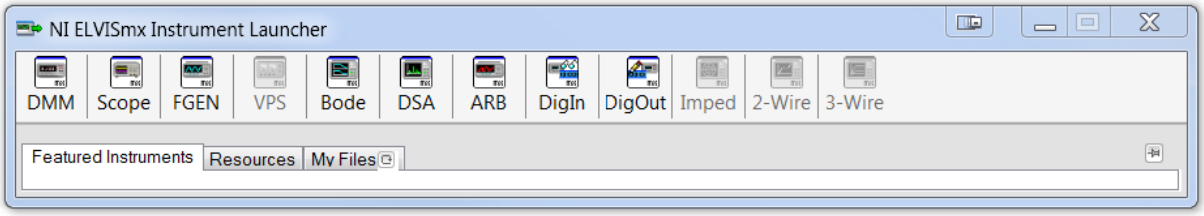
The following set of instructions demonstrates the use of the myDAQ to measure characteristics of a simple RC circuit on the DMS.



59. Using a resistor and capacitor, create the following circuit.
    This example uses a 10k resistor and 10 nF (.01 µF) capacitor.
    a. Analog Output (AO) Channel 0 = Blue
    b. Analog Input (AI) Channel 0 = Orange
    c. Analog Input (AI) Channel 1 = Green
60. Navigate to:

    Program -> National Instruments -> NI ELVISmx for NI myDAQ -> NI ELVISmx Instrument Launcher

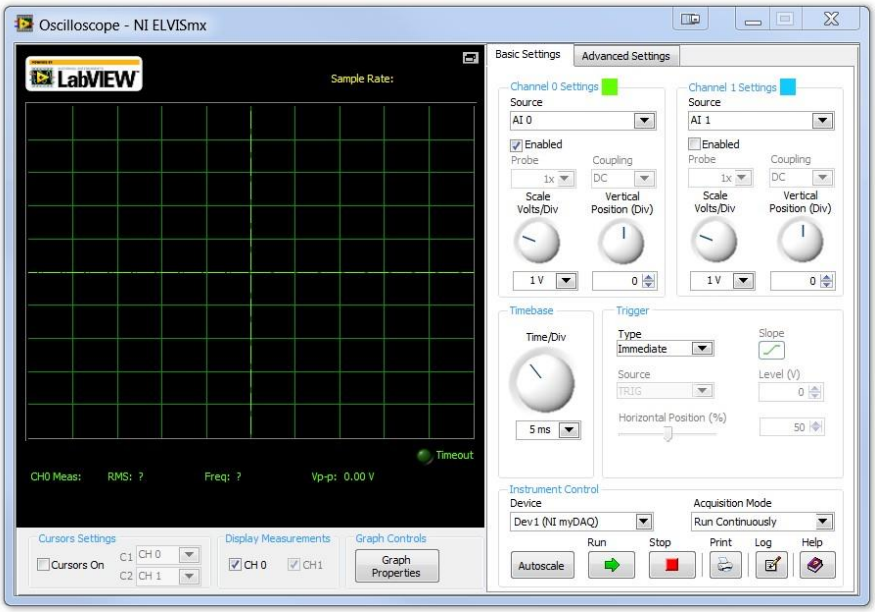
61. Open "**NI ELVISmx Instrument Launcher**".

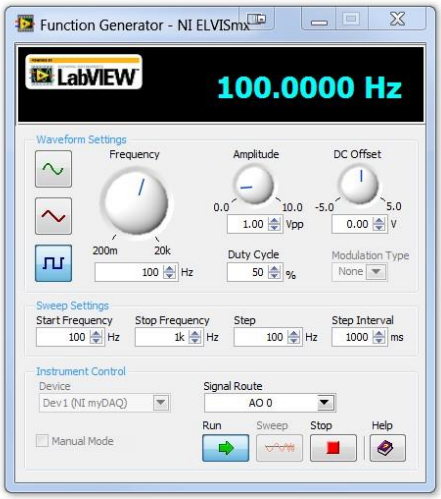


Function Generator (FGEN) and Oscilloscope (Scope)

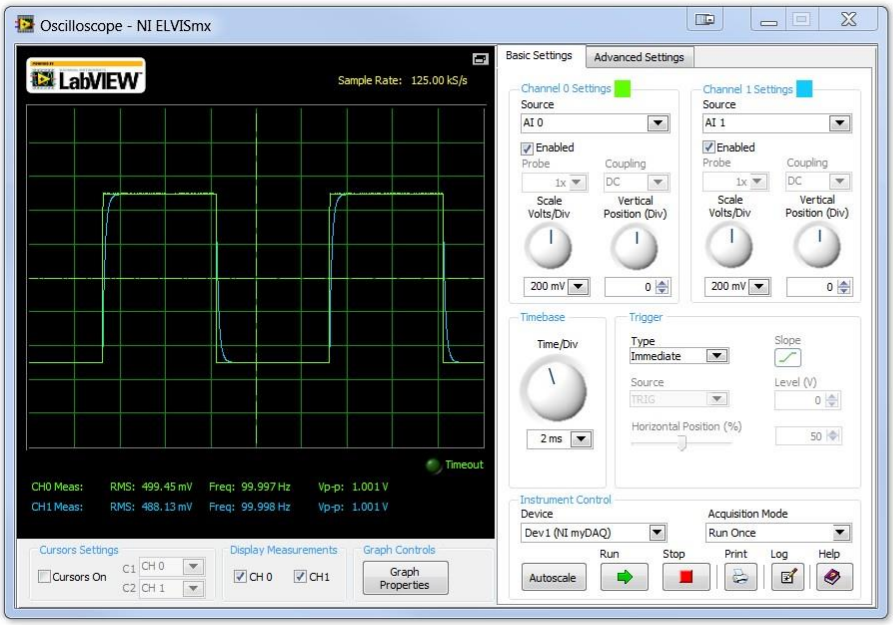
In this demonstration, we will use the function generator to generate a signal and the oscilloscope to compare this signal with the circuits output signal.

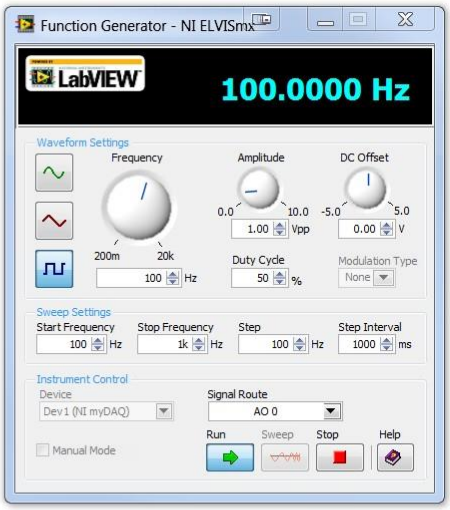
62. Open: **FGEN** and **Scope.**





63. **Function Generator (FGEN) Settings:**
    a. Waveform Settings: **Square**
    b. Select: **Run**
64. **Oscilloscope (Scope) Settings:**
    a. Channel 0 Settings:
        i. Source: AI 0 (This is the CLK signal from FGEN) **Check: Enabled**
        ii. Scale Volts/Div: 200 mV
    b. Channel 1 Settings:
        i. Source: AI 1 (This is the output of the circuit) **Check: Enabled**
        ii. Scale Volts/Div: 200 mV
    c. Timebase: Time/Div: 2 ms
    d. Instrument Control:
        i. Acquisition Mode: **Run Once**





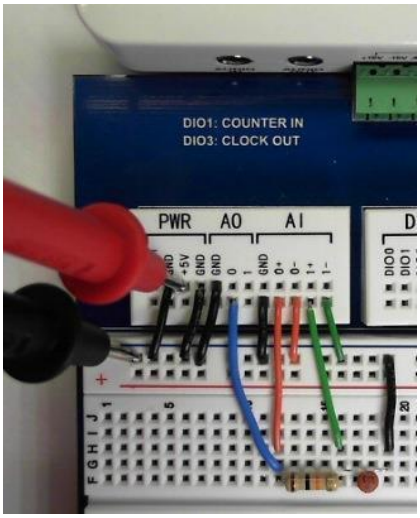
The green trace is the waveform coming from the function generator. The blue trace is the output from the RC circuit. If you are using a resistor or capacitor with a different value you will need to adjust the Timebase and Volt/Div Scale so that the trace fits in the display.

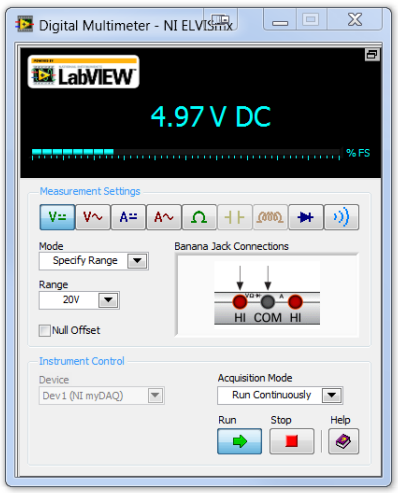
Digital Multimeter (DMM)

The Digital Multimeter (DMM) allows students to measure Current, Voltage, and Resistance.

In this demonstration, we will use the DMM to measure output voltage provided by the myDAQ to the myDigital Protoboard. The DMM is fused for protection when reading current.

65. Open: **DMM**
66. **DMM Settings**:
    a. Measurement Settings:
        i. DC Voltage
        ii. Range 60V
67. Make sure the Banana Jack Connection match the diagram and they touching the +5V and GND on the DMS as pictured.
68. Select : **Run**
69. Change the Range to 20V and note the difference.
70. Change the Range to 2V and note the difference. Switch back to 20V range.





Optional Support: Digital Logic Board (DLB)

NI DEFB Driver Installation for use with the Digital Logic Board (DLB)

The following instructions describe the installation process on the NI DEFB Driver for use on the Digital Logic Board in your classroom. If using the DMS and DLB, each board requires a different driver.

1. Download and install: **DEFB Driver** (32 and 64-bit). The **DEFB Driver** can be located in the **Virtual Academy Here**: (Access available only after completion of CT.)

   Technical Support & Software Downloads-->
   Pathway To Engineering ->DE->Optional->FPGA Drivers 32/64

2. Once downloaded, extract the driver files and run setup.exe. Follow the prompts to install and upon completion, reboot the machine.

3. Plug the DLB into a USB port on your computer and power it on. With your speakers turned on, you will hear the USB port chime on and off a few times.

   a. For 32-bit XP users, the driver wizard will pop up three times. The path to the driver is: **C:\Program Files\National Instruments\FPGA.**

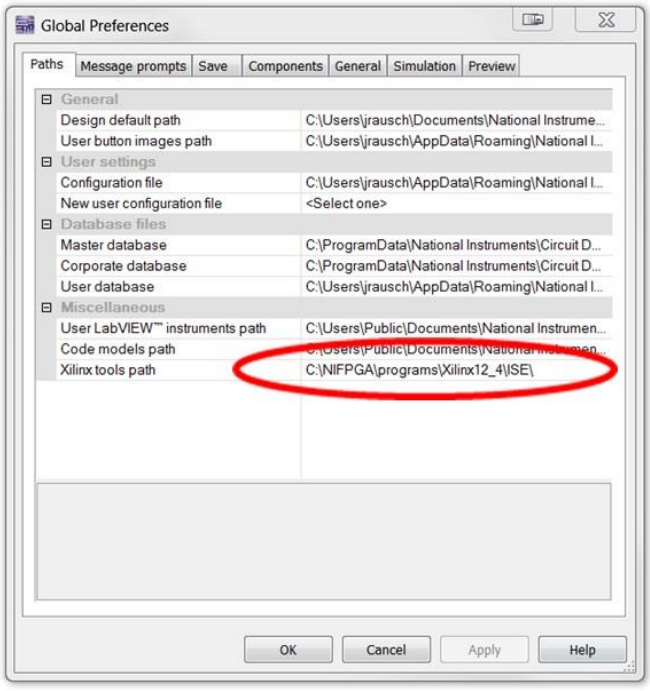
Digital Logic Board (DLB): Transfer → Export to PLD Process

4. Download and open "**External Clock Test (DLB_12.4)**" in Multisim.

5. Connect the DLB to your computer with the USB cable if not already connected.

6. Once the selected test file is open:

   Select: Options -> Global preferences -> Paths -> Miscellaneous -> Xilinx tool path. Make sure the **Xilinx tool path** is set to **C:\NIFPGA\programs\Xilinx12_4\ISE.**



7. Select: **Transfer -> Export to PLD.** This will bring up a menu. Select: **Next**
8. Xilinx tool:

   Under the Xilinx tool drop down menu select:

   Xilinx ISE Design Suite 12.4 32-Bit or Xilinx ISE Design Suite 12.4 64-Bit

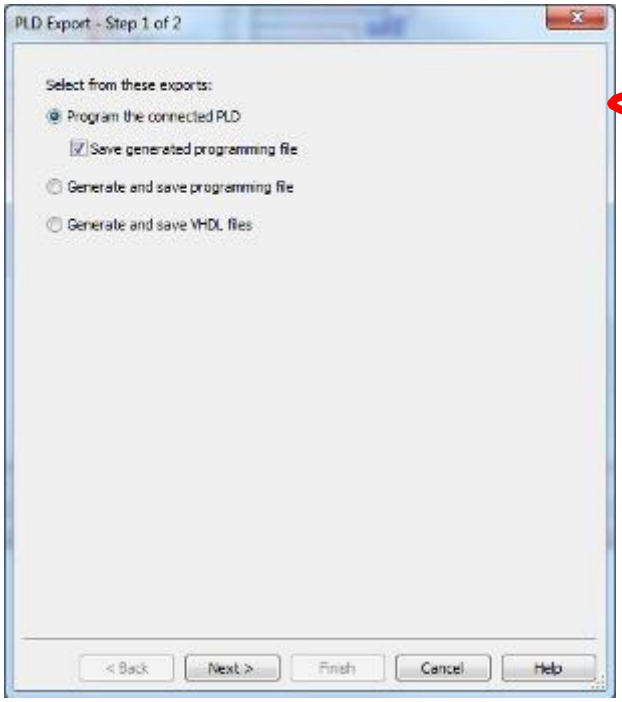


Figure A

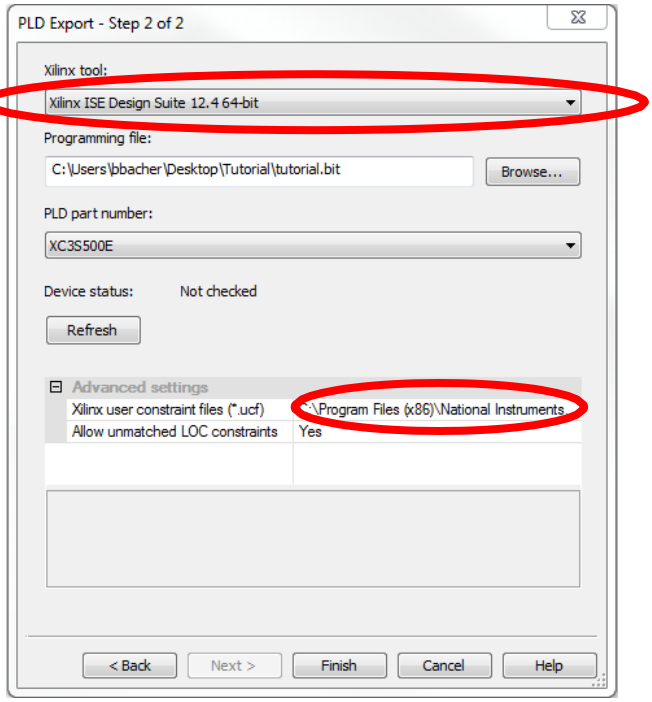


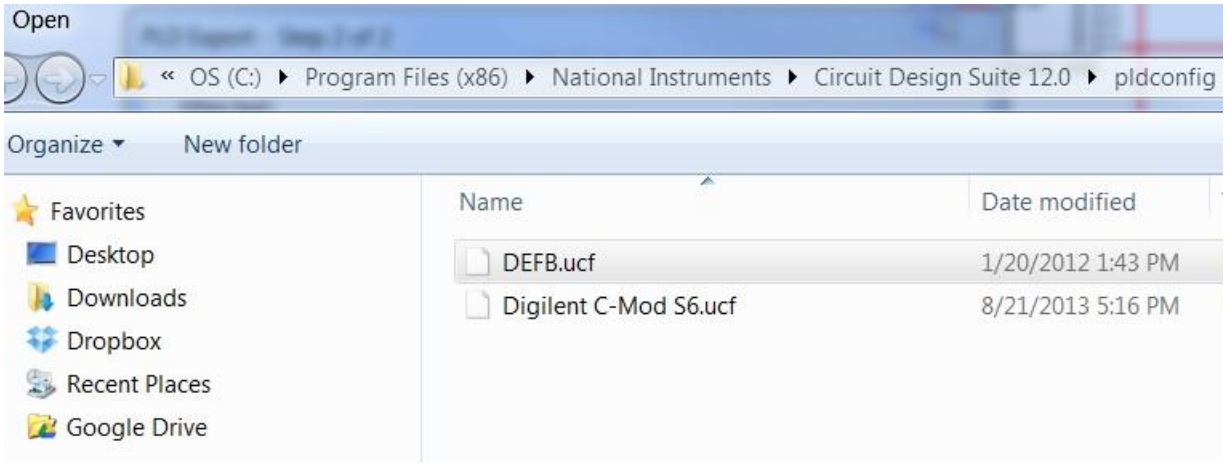
Figure B

Programming file: Select Browse: Set your location for the programming file if you are not already there.

PLD part number: The PLD part number will auto-populate.

Advance settings: Under the advanced settings click the button on the right side of the Xilinx user constraint files row. Navigate to and select “DEFB.ufc” from pldconfig folder.

Xilinx user constraint files (*.ufc): Set path to
C:\Program Files\National Instruments\Circuit Design Suite 12.0\pldconfig



9. Allow unmatched LOC constraints needs be set to yes.
10. Click finish.
11. Exporting to the PLD will take several minutes. If the device is not found:
    - Check that the USB cable is connected.
    - Check user constraint path under PLD export Step 2.
    - Check the Xilinx tool path under Global Settings.
    - Check your Device Manager to see if “Digilent USB Device” is found.
12. With RotCLK wired to GPIO0 you should be a count of 0-60 on the Seven-Segment Displays. You can change the rate using ROT1