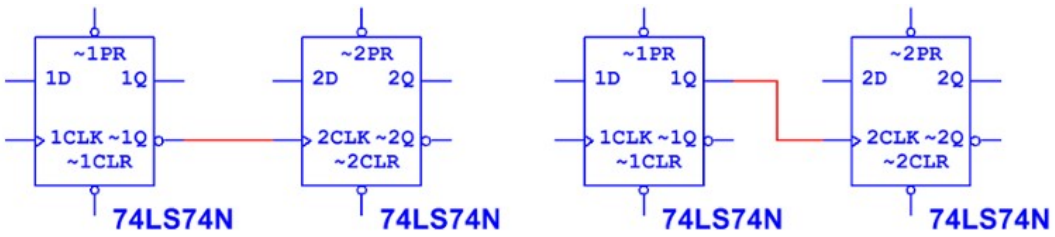
Activity 3.2.1

Asynchronous Counters: Small-Scale Integration (SSI) Up/Down Counters Using PLTW S7

INTRODUCTION

Asynchronous counters can be designed to count up or count down using Small-Scale Integration (SSI). The small-scale design can use almost any flip-flop type. To observe this process, we will simulate and analyze multiple 3-bit counters based on both D and J/K flip-flops. For both the D flip-flop and J/K flip-flop, we will modify circuits so that they count up or count down. Remember, for **up counters** , connect the CLK to the Q output of the opposite polarity. For **down counters,** connect the CLK to the Q output of the same polarity.

SSI (D flip-flops)



Opposite Polarity = Up Counter **Same Polarity = Down Counter**

EQUIPMENT

- Circuit Design Software (CDS)
- Digital MiniSystem (DMS)
  - myDAQ
  - myDigital Protoboard
  - PLTW S7 FPGA Module
- #22-gauge solid wire

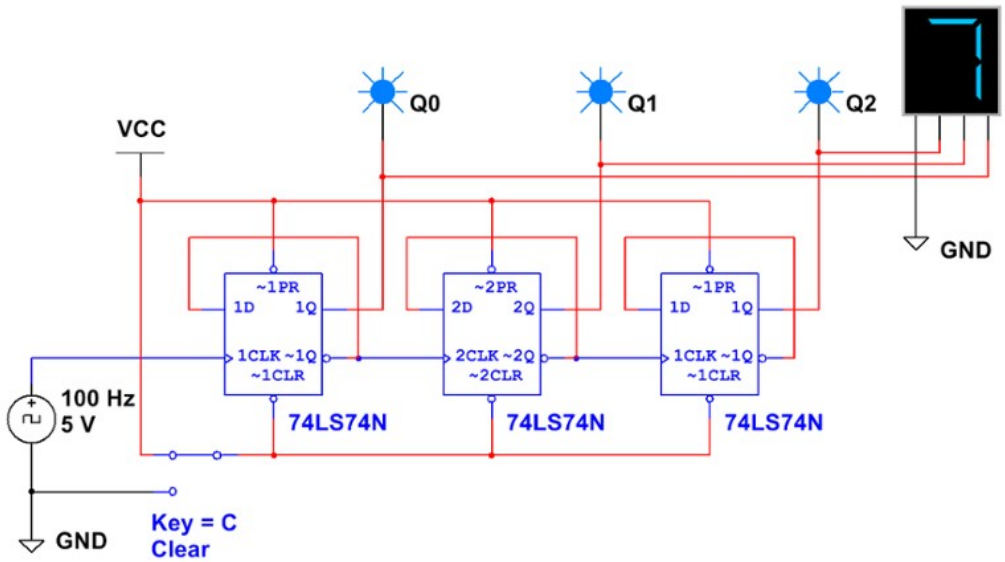
RESOURCES

Asynchronous Counter Using PLTW S7

Procedure

Simulation (Design Mode)

1. The circuit shown below is a 3-Bit Binary-Up Counter implemented with 74LS74 D flip-flops. This design counts from 0 to 7 and then repeats.



3-Bit Binary Up Counter with D Flip-Flops

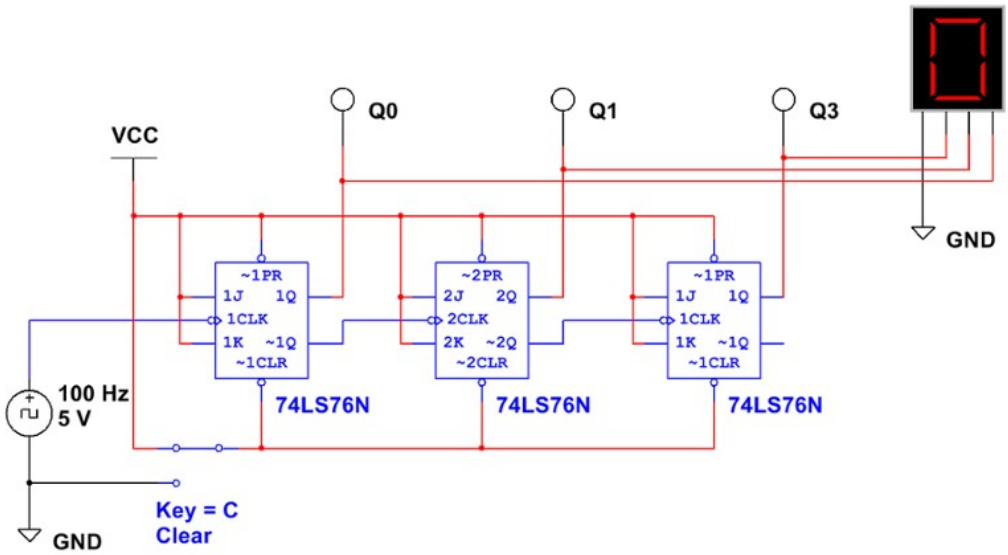
   a. Using Design Mode of the CDS, enter the 3-Bit Binary Up Counter.
   b. With the RESET switch set to 5V, start the simulation. Verify that the circuit is working as expected. If the results are not what you expected, review your circuit and make necessary corrections. You may need to adjust the clock speed to be able to observe the outputs changing.
   c. With the simulation running, toggle the RESET switch to GROUND. What effect does this have on the output?
   d. Toggle the RESET switch back to 5V. What effect does this have on the output?
   e. Observe that the HEX DISPLAY appears to jump between some count changes. What causes this to occur?

2. Modify the circuit in step 1 to make it a 3-Bit Binary Down Counter.

Repeat steps 1a through 1e for this modified counter.

a. Using Design Mode of the CDS, enter the 3-Bit Binary Down Counter.
b. With the RESET switch set to 5V, start the simulation. Verify that the circuit is working as expected. If the results are not what you expected, review your circuit and make any necessary corrections. You may need to adjust the clock speed to be able to observe the outputs changing.
c. With the simulation running, toggle the RESET switch to GROUND. What effect does this have on the output?
d. Toggle the RESET switch back to 5V. What effect does this have on the output?

3 The circuit shown below is a 3-Bit Binary Down Counter implemented with 74LS76 J/K flip-flops. This design counts from 7 to 0 and then repeats.



3-Bit Binary Down Counter with J/K Flip-Flops

a. Using Design Mode of the CDS, enter the 3-Bit Binary Down Counter.
b. With the RESET switch set to 5V, start the simulator. Verify that the circuit is working as expected. If the results are not what you expected, review your circuit and make necessary corrections. You may need to adjust the simulation speed to be able to observe the outputs changing.
c. With the simulation running, toggle the RESET switch to GROUND. What effect does this have on the output?

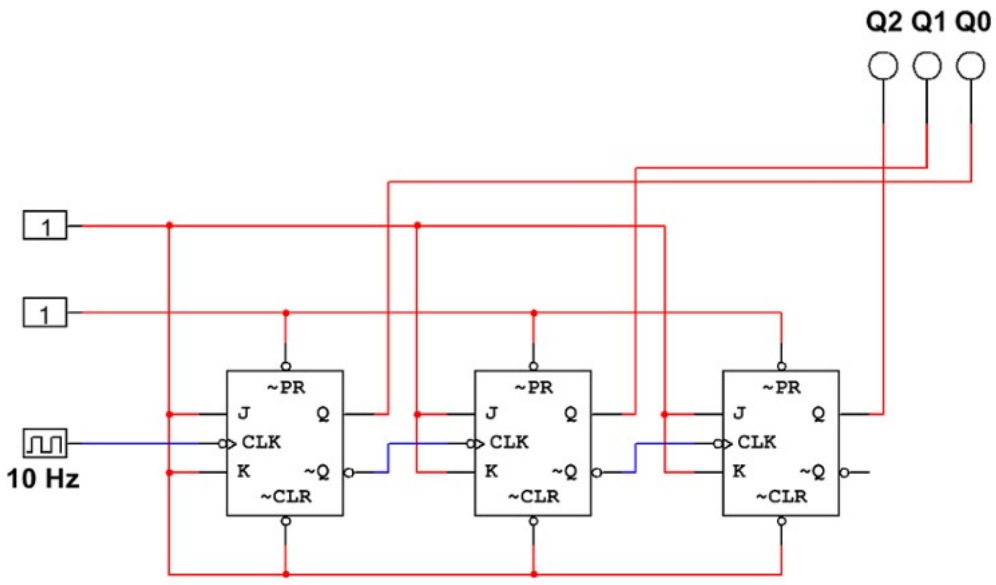
d. Toggle the RESET switch back to 5V. What effect does this have on the output?

4 Modify the circuit in step 3 to make it a 3-Bit Binary Up Counter.
Repeat steps 3a through 3d for this modified counter.

a. Using Design Mode of the CDS, enter the 3-Bit Binary Up Counter.
b. With the RESET switch set to 5V, start the simulator. Verify that the circuit is working as expected. If the results are not what you expected, review your circuit and make necessary corrections. You may need to adjust the simulation speed to be able to observe the outputs changing.
c. With the simulation running, toggle the RESET switch to GROUND. What effect does this have on the output?
d. Toggle the RESET switch back to 5V. What effect does this have on the output?

Simulation (PLD Mode)

5 The circuit below is the same 3-Bit Binary Down Counter implemented with 74LS76 J/K flip-flops (only it is created in PLD Mode).
This design will count from 7 to 0 and then repeat.



3-Bit Binary Down Counter with J/K Flip-Flops

a. Using PLD Mode of the CDS, enter the 3-Bit Binary Down Counter.
b. Change the circuit so that the 3-Bit Binary Down Counter will reset to seven (111).

Export to PLD (PLD Mode)

c. Assign the inputs/outputs in PLD mode and wire the circuit using the DMS.
   - Assign **Reset to (111)** to a push button.
   - Assign **(D0-D2)** to 3 LEDs of the same color in a row.
d. Verify that the design works on your DMS.

CONCLUSION

1. Explain why asynchronous counters are also referred to as ripple counters.

2. What changes must be made to a 3-Bit counter to make it a 4-Bit counter?

3. The RESET circuit used on the four 3-Bit Counters analyzed in this activity reset the counts to zero (000). It makes sense for the up-counters to start at zero (000), but the down-counters should start at seven (111). What would you need to change so that the 3-Bit Binary Down Counter with J/K Flip-Flops you just created would reset to seven (111)?