Activity 3.3.2

Synchronous Counters: Medium-Scale Integration (MSI) 74LS163 Up Counter Using PLTW S7

INTRODUCTION

Several Medium-Scale Integrated (MSI) Circuit counter chips are available to digital designers who need a binary **up counter** as part of their new design. Each of these ICs has their own unique set of features. Matching these features to the needs of the design will determine which IC is best suited for the particular application.

For the sake of time in this activity, we will limit our designs to the 74LS163 Synchronous 4-Bit **Binary Counter** IC. There is no feature that makes this particular counter better than the others; it is just a representative sample of the different MSI counter ICs available.

A unique feature for 74LS163 is that the LOAD is a synchronous input. This means the data input will be loaded into the counter on the next rising edge of the clock when the LOAD input is a logic (0). In previous designs, the “reset” was defined as the count plus 1 for up counters, and the count minus 1 for **down counters** . For the 74LS163, the “reset” is defined by the count limit. (Example: if the desired count range is 2 to 7, the LOAD “reset” is wired for the number 7. The number “7” will display, and the count will reset or LOAD on the transition from 7 to 8.

In this activity we will simulate and build counters that were designed using the 74LS163 Synchronous 4-Bit Binary Counter IC.

EQUIPMENT

- Circuit Design Software (CDS)
- Digital MiniSystem (DMS)
  - myDAQ
  - myDigital Protoboard
  - PLTW S7 FPGA Module
- or Digital Logic Board (DLB)
- #22-gauge solid wire

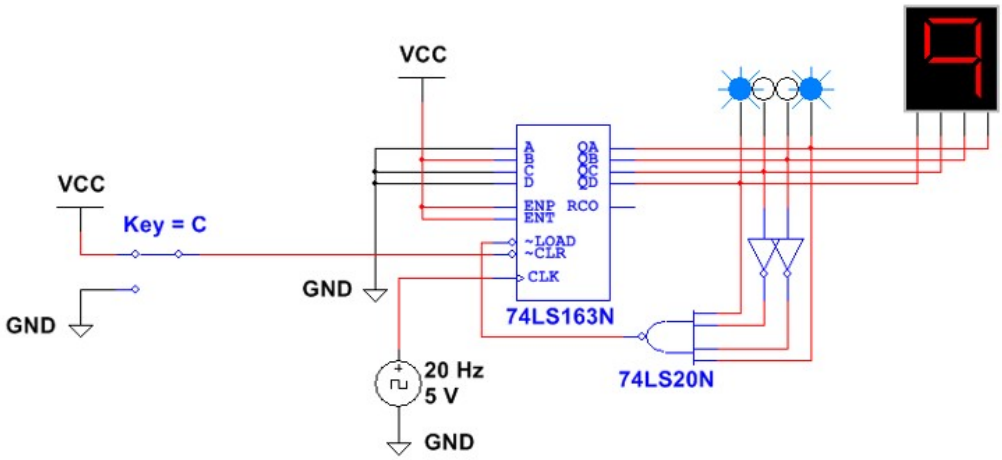
RESOURCES

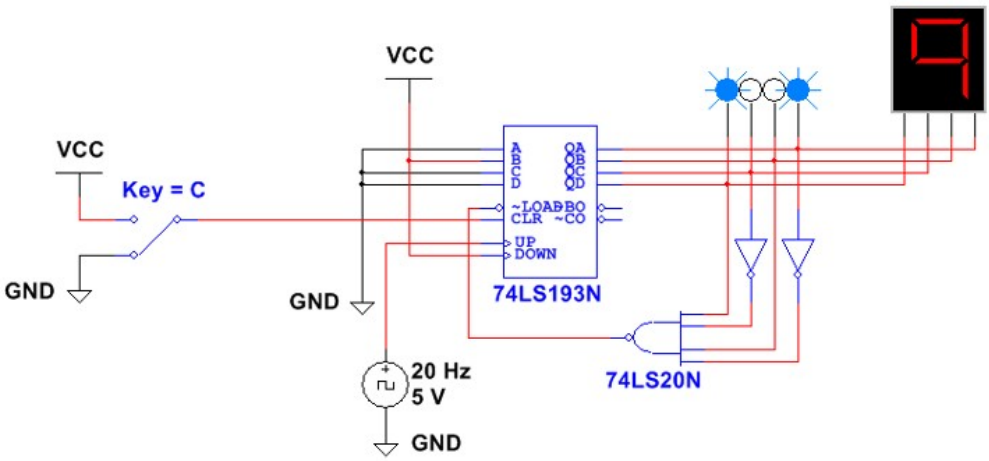
Synchronous Counters with MSI Gates Using PLTW S7

Procedure

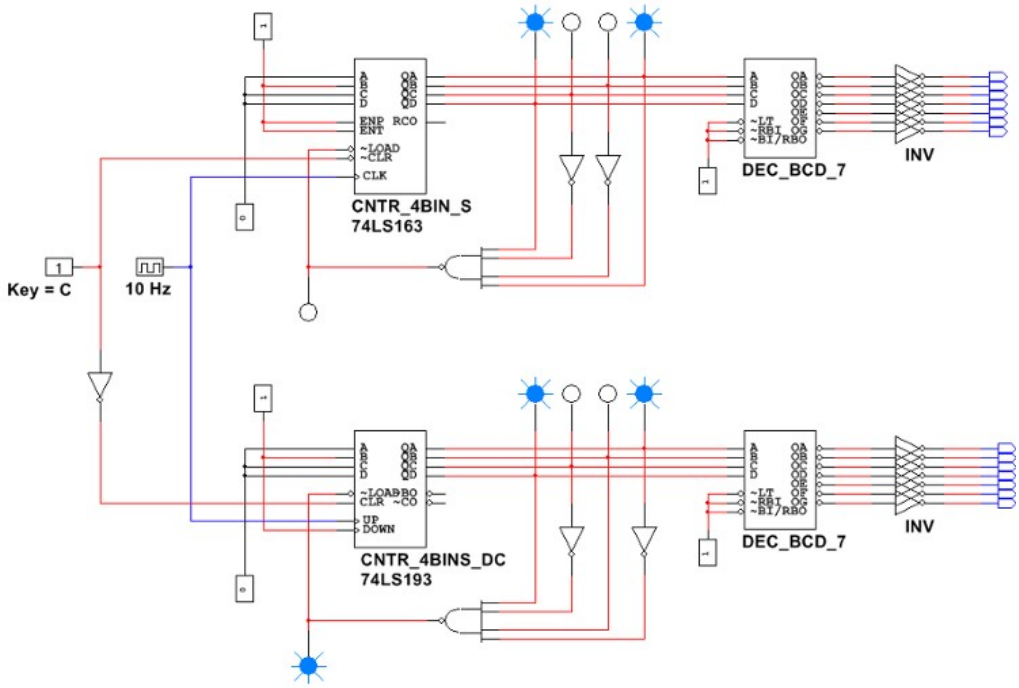
Simulation (Design Mode)

1. Below are two MSI **Synchronous Counters** created in design mode of the CDS. They are the 74LS163 Up Counter with synchronous load and the 74LS193 **Up/Down Counter** with asynchronous load.



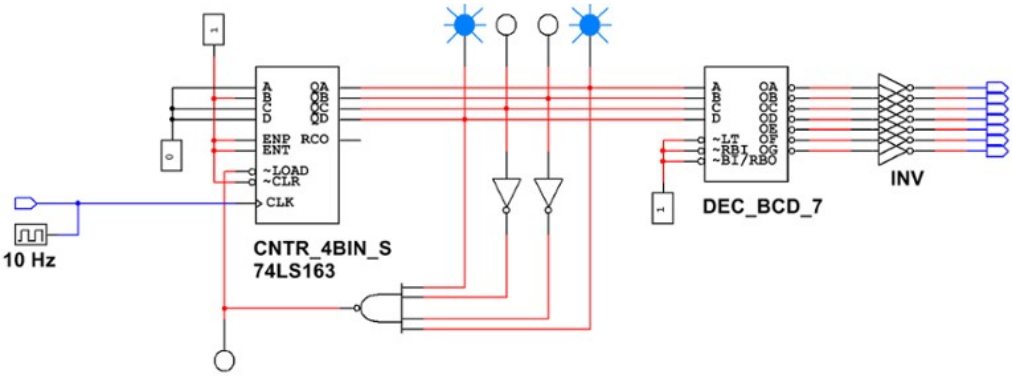


2. Each of these MSI counters has a corresponding representation in PLD Mode.



Simulation (PLD Mode)

3 The circuit below is a 4-Bit Binary Up Counter designed to count from 2 to 9. This counter is designed with the PLD Mode version of the 74LS163 MSI Counter IC.



4 Using the CDS, enter the 2 to 9 Binary Up Counter in PLD Mode. By monitoring the logic probes attached to outputs QD, QC, QB, and QA, verify that the circuit is working as expected (Is the count 2 to 9?). If the

results are not as expected, review your circuit and make necessary corrections.

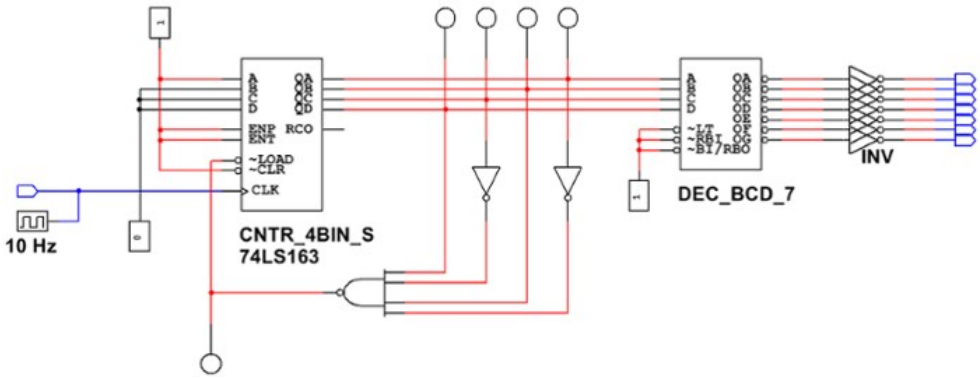
a. Make the necessary modification to the counter design to change the count to 4 to 14. Using the CDS, verify that the circuit is working as expected. If the results are not as expected, review your circuit and make necessary corrections.
b. Using the DMS, build and test the 4 to 14 counter that you designed and simulated in step 4a. Verify that the circuit is working as expected and that the results match the results of the simulation.

CONCLUSION

1. What are the advantages of implementing a synchronous counter with the 74LS163 integrated circuit versus using discrete flip-flops and gates?

2. In previous counters that you have created, you set the upper limit as the value just past the last digit you wanted displayed. That is not the case with this design. Why is the way you set the range different for this design?

3. Analyze the counter shown below to determine the counter's lower and upper count limit.



Proceed to next activity