Activity 3.3.3

Synchronous Counters: Medium-Scale Integration (MSI) 74LS193 Up/Down Counter Using PLTW S7

INTRODUCTION

In the last activity, we began our study of MSI **synchronous counters** by examining the 74LS163 Synchronous 4-Bit **Binary Counter** IC. While this IC works for many applications, it lacks one feature. The 74LS163 functions only as an **up counter**. If your design calls for a **down counter**, that IC will not work.

For applications that call for a down counter, the 74LS193 Synchronous 4-Bit Binary Counter IC is the IC of choice.

In this activity we will simulate and build counters designed using the 74LS193 Synchronous 4-Bit Binary Counter IC.

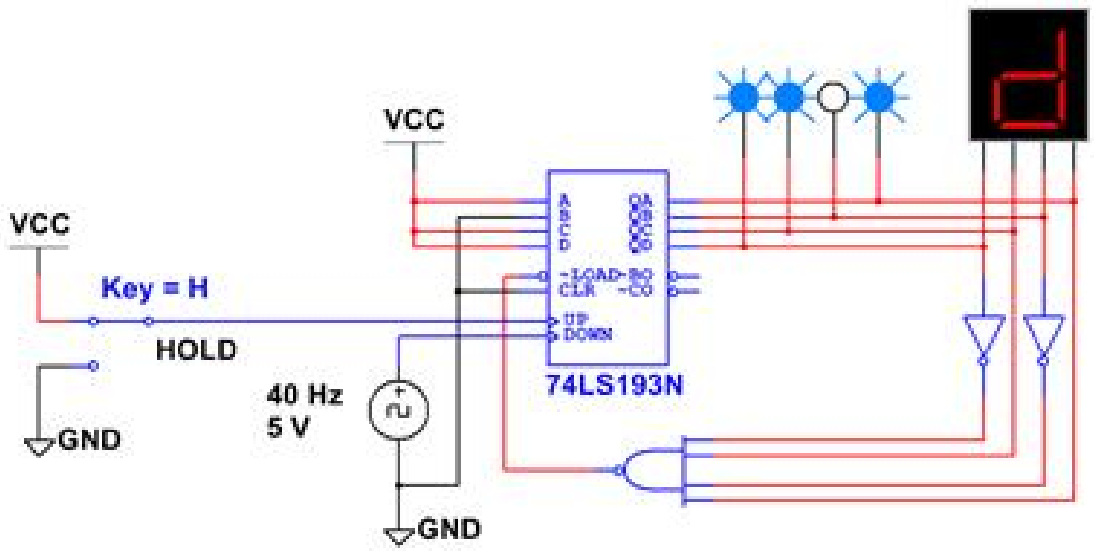
EQUIPMENT

- Circuit Design Software (CDS)
- Digital MiniSystem (DMS)
  - myDAQ
  - myDigital Protoboard
  - PLTW S7 FPGA Module
- #22-gauge solid wire

Procedure

Design Mode

The circuit below is a 4-Bit Binary Down Counter created in Design Mode.
It is designed to count from 13 to 6 with the 74LS193 MSI Counter IC.



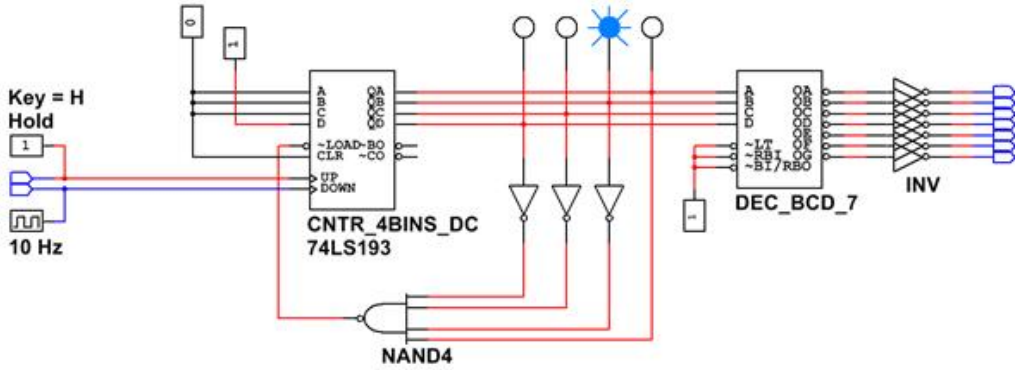
13 to 6 Binary Down Counter

1. Using Design Mode of the CDS, enter the 13 to 6 Binary Down Counter. By monitoring the logic probes attached to outputs QD, QC, QB, and QA, verify that the circuit is working as expected (Is the count 13 to 6?). If the results are not as expected, review your circuit and make any necessary corrections.

2. Using Design Mode of the CDS, make the necessary modification to the counter design to change the count to 6 to 13 Binary Up Counter. Verify that the circuit is working as expected. If the results are not as expected, review your circuit and make necessary corrections.

PLD Mode

4 The circuit shown is a 4-Bit Binary Down Counter created in PLD Mode. It is designed to count from 8 to 2 with a CNTR_4BINS_DC, which is the PLD equivalent of the 74LS193 in Design Mode.



a. The CNTR_4BINS_DC (PLD Mode version of the 74LS193) is a Synchronous 4-Bit Binary **Up/Down Counter** with two Clocks.
b. The two Clocks are designed to receive *only* clock signals. You cannot tie the UP or DOWN to a 1 or 0.
c. If creating this circuit in PLD Mode, you *must* connect the Down count (Hold) to a switch or an input of 5V.

5 Using PLD Mode of the CDS, enter the 8 to 2 Binary-Down Counter. By monitoring the logic probes attached to outputs QD, QC, QB, and QA, simulate and verify that the circuit is working as expected (i.e., Is the count 9 to 2?). If the results are not as expected, review your circuit and make any necessary corrections.

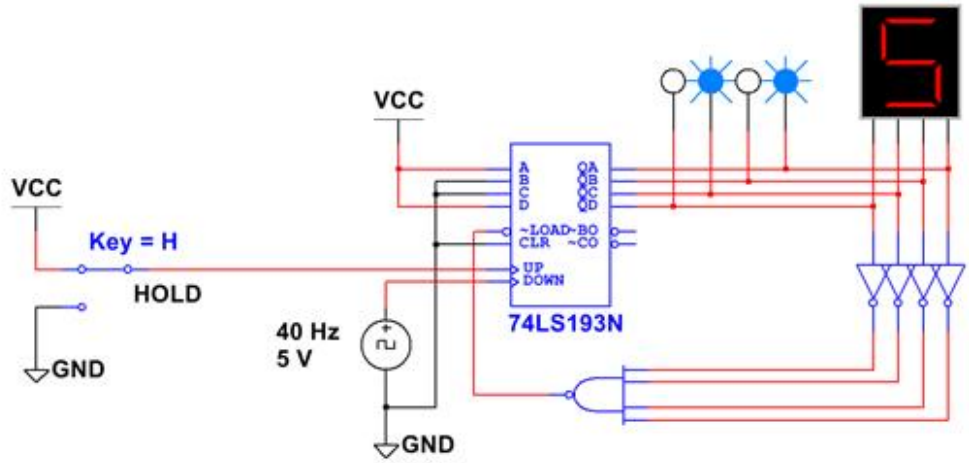
6 Using PLD Mode of the CDS, make the necessary modification to the counter design to change the count to 2 to 8 Binary Up Counter. Export the design to your PLD and verify that the circuit is working as expected.

CONCLUSION

1. What are the advantages of implementing a synchronous counter with the 74LS193 IC over the 74LS163 IC?

2. What is the difference between a synchronous load input (74LS163) and an asynchronous load input (74LS193)?

3. Analyze the counter shown below to determine the counter's lower and upper count limit.



Proceed to problem