Problem 3.3.4

Synchronous Counters: Sixty-Second Timer Using PLTW S7

INTRODUCTION

In this design problem, you have the opportunity to draw together all of the concepts and skills that you have developed pertaining to **synchronous counter** design. You will design, simulate, and create a Sixty Second Timer.

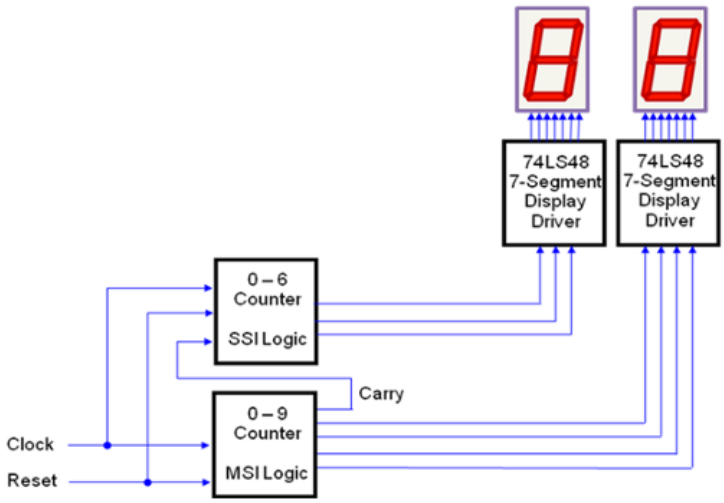
EQUIPMENT

- Circuit Design Software (CDS)F
- Digital MiniSystem (DMS)
  - myDAQ
  - myDigital Protoboard
  - PLTW S7 FPGA Module
- #22-gauge solid wire

Procedure

Design (Sixty-Second Timer)

Design a digital Sixty-Second Timer that counts from 00 to 59. This design has two control inputs and two output displays. The two inputs are **Clock** and **Reset**. The **Clock** signal is a 1 Hz square wave that controls the count rate. The **Reset** signal, when it is a logic zero, resets and holds the count at zero. When the **Reset** signal is a logic 1, counting is enabled. When the count reaches sixty seconds, the counting resets at 0.



Design Specifications

- The two output displays are common cathode seven-segment displays that require a multiplexed signal.
- Each display will use a 74LS48 BCD-to-Seven-Segment display driver in Design Mode. (DEC_BCD_7 in PLD Mode)
- The ones-unit display (0–9) is controlled by a synchronous counter designed with a 74LS163 MSI counter IC. (CNTR_4BIN_S in PLD Mode)

- The tens-unit display (0–6) is controlled by a synchronous counter designed with SSI logic gates (J/K).
- Any additional logic may be used as needed to support the counter designs.

Simulation (Design Mode or PLD Mode)

Using the Circuit Design Software (CDS) enter and test your Sixty Second Timer design.

- Design Mode Option: If you choose to create the circuit in Design Mode to simulate, remember that you will need to recreate the circuit in PLD Mode to prototype the circuit.
- PLD Mode Option: To bypass the need to recreate the circuit a second time, you can create and simulate the circuit in PLD Mode. Just remember that you will not have an SSD for simulation in PLD Mode. You will need to use probes to track the counts and events.

Verify that the circuit is working as designed. If not, review your design work and circuit implementation to identify your mistake. Make necessary corrections and retest. Be sure to document all changes in your engineering notebook.

Prototyping

Using the Digital MiniSystem (DMS), export your Sixty-Second Timer design to the PLTW S7 PLD Module. Verify that the circuit is working as designed. Remember to use PIO16 for a clock signal. If your circuit isn't working correctly, review your circuit implementation to identify mistakes, make the necessary corrections, and retest. Be sure to document all changes in your engineering notebook.

CONCLUSION

Using your engineering notebook as a guide, write a conclusion (minimum 250 words) that describes the process that you used to design, simulate, and build your Sixty Second Timer circuit. This conclusion must include all of your design work, preliminary and final schematics, parts list, and a digital photograph of your final circuit. The documentation should be complete enough that another student, with the same knowledge of digital electronics, could reproduce your design without any additional assistance.

Proceed to next unit